EDN europe

Conductive inks make tracks in product mouldings

TACTOTEK™

pulse

designideas
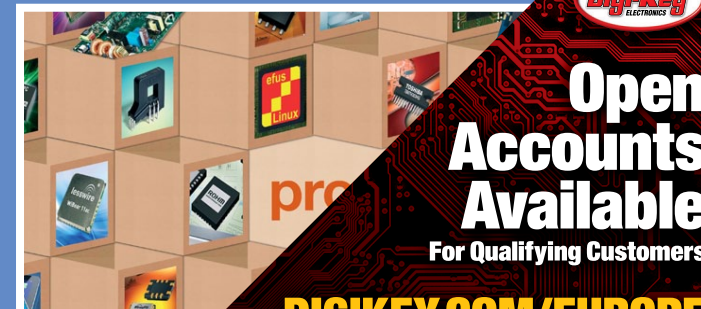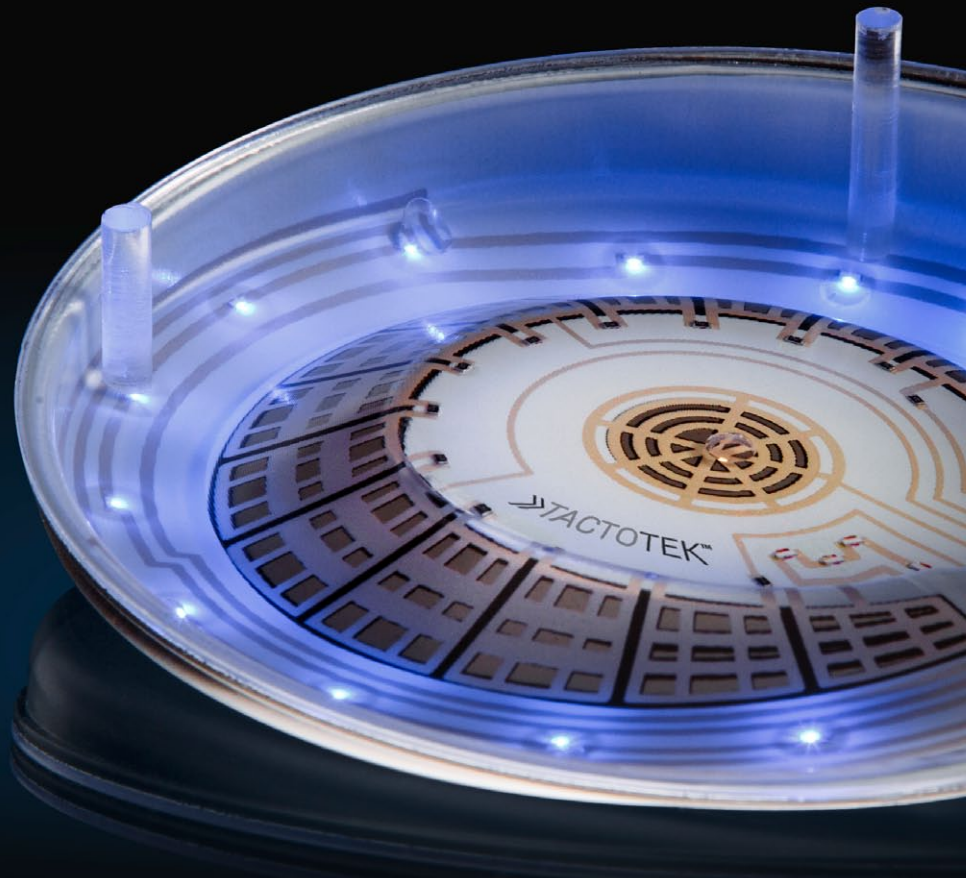
The World's Largest Selection of Electronic Components Available for Immediate Shipment!™

We Source What's Inside
YOUR DESIGN

COVER

Conductive inks print circuits in moulded parts

DuPont Microcircuit Materials is introducing a range of in-mould electronic inks, that increase the variables for mechanical and electronic designers, and aid functional integration.

The suite of in-mould electronic inks is designed to help streamline electronic devices by reducing the need for rigid circuit boards. By printing circuits directly onto plastic substrates, touch controls – such as electronic buttons, switches and slides – are readily integrated in applications such as home appliances and cars. The inks offer design, manufacturing, weight and cost advantages and mark the further expansion of DuPont advanced materials enabling printed electronics. The image shows a reference design using integrated printed circuitry that is enabled by DuPont ME series in-mould electronic inks. (Photo by TactoTek [Oulu, Finland]).

The DuPont ME series in-mould electronic inks are designed to withstand demanding manufacturing processes such as thermoforming and injection moulding. They also simplify the assembly process because there is only a single connection point and no wires behind the console. This can reduce the weight of a console by more than 70%. In addition to increased design freedom and lighter weight, the technology can reduce cost by up to 50% compared to currently available buttons and up to 20% versus other electronic touch switch systems. More here.

FEATUREARTICLES

ONLINE THIS MONTH

EDN's columns

COUNSEL OF PERFECTION

Given the chance to restructure, from first principles, the process of creating embedded software, how would you change the way things are done? Here are a few thoughts... In our ideal world we will start by describing the functions we require, in plain language: to that we can add the list of things our system must not do. Both should then be expressed in, or transformed into, a form close to plain language: but one that is comprehensible, with precisely-defined meanings, to a software tool. This is the stage at which most, if not all, simulation should take place, modifying and refining the description until the simulated operation corresponds to the system architects' intent.

The next stage would be to take the same description – without any changes – and feed it into a code generator... and, thereafter, to each stage that we currently pass developing software through. But with the condition that each tool should be automated and that no design changes are permitted on the work-in-progress, until an executable is reached. Any changes required are to be carried out at the top level, re-verified, then progressed through the complete chain; each step being rule-based, correct-by-construction and readily verifiable by formal tools.

That, of course, is a wildly simplistic view of how-things-might-be. However, contrast it with what actually happens; a full verification of a [near] plain-language description is uncommon; we quickly dive into coding, and much of the design intent is translated into function at the coding stage. Certainly, there are modelling languages, and specification languages – but the majority of the work done there is effectively thrown away, in the sense that coding frequently starts by re-interpreting the system description. A description in a specification language may be used as a testbench to verify the design late in the cycle – but by that time all manner of mayhem may have been wrought on the original intent.

Coding is an immensely powerful process, with virtually unlimited degrees of freedom, where skilled people can do very creative things. Probably for that reason, it has come to be seen as a creative process, whereas (arguably) it is not, or should not be; it is essentially mechanical, a step in translation from design intent to executable. In our Utopia we can say; if you are applying creativity in coding, you are doing so too late. Human interpretation, via a very flexible medium, of a design specification affords great scope for ambiguities and errors. Hence, the vast amount of ingenuity that is applied to writing checking and verification tools to trap those bugs.

Why do we not have tools (in general use, that is) that will generate bug-free code from a high-level description? Partly, of course, because it's hard; but also (let me contend) because the very people who might otherwise be beating on the door of Computer Science demanding a more sophisticated methodology are the same community that rejects any move in that direction, and treats any automatically-generated code with suspicion, if not outright contempt.

The temptation to draw a parallel with the development of hardware (silicon IC) design is irresistible. Not that every step along the way from schematic capture, to RTL, to VHDL, to packaged IP, has arrived unopposed. However, if the hardware design community had rejected shifts to designing at a higher level of abstraction to the extent that the software world has, it is highly unlikely that any of today's complex SoCs would ever be completed at all. Part of the reason for that success is that semiconductor designers have accepted – or have been forced to accept – a constrained design space. In simple terms; limit yourself to doing only the things that the automated tools do well, and you will make rapid progress. There's a saying, related to project delivery schedules and engineers' instinct for perfection, "I don't want it perfect, I want it Friday". By analogy, in today's climate, software that is smart, and compact, and – for lack of better term, 'cool' - is seen as desirable. The alternative, that you might express as, "I don't want it cool, I just want it correct," might have something to add to today's approach.
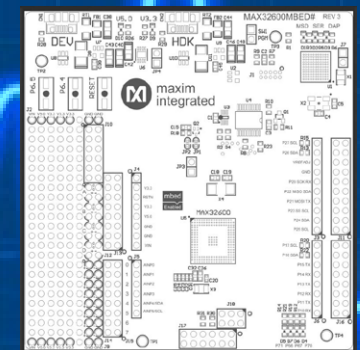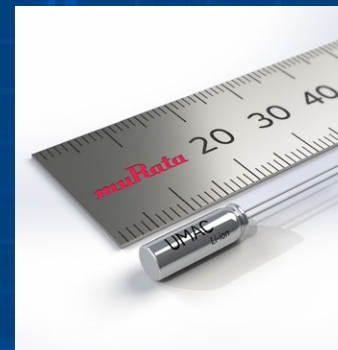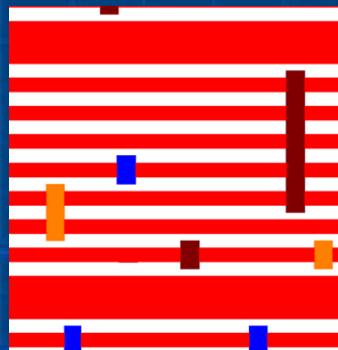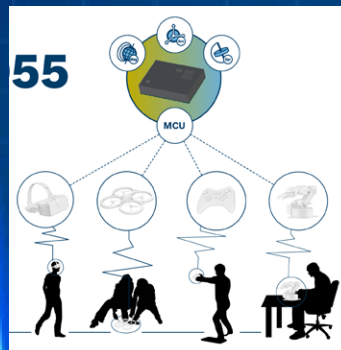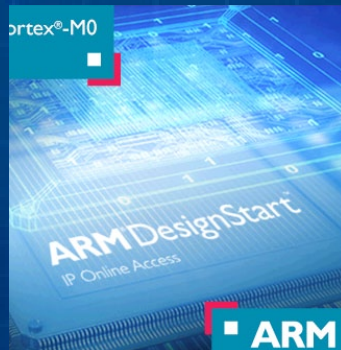
Bake your own Pi – element14 & Raspberry Pi set up path to customised Pi

Designers and engineers creating or building products based around the Raspberry Pi, in
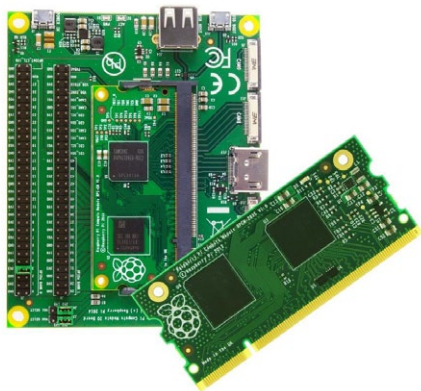
small-to-medium volume, can now access a service set up by distributor element14, and Raspberry Pi Trading to design and manufacture customised versions of the Pi. As before, the software of the Pi is open source, but the hardware is proprietary; areas that might be considered for customisation would include configuration of the PCB, adding functions, re-designing interfaces or headers/pinouts, and altering memory configurations. The core (Broadcom) silicon

and its immediate circuit context is not available to be changed; the same is true of the power supply configuration around the processor, where a substantial amount of work has been invested to achieve the board's performance. element 14 anticipates that typical projects will be in the 3000-5000 volume range; but that is very flexible. The Foundation's Eben Upton says that he expects to see many projects in the 100-1000 initial production range to be enabled by this move: he sees it as the next step from what many users have been doing with the compute module variant of the Pi (pictured). Most projects, the partners expect, will have been 'prototyped' on existing hardware, but element 14 says it could take a project from an earlier 'concept' stage. All current variants of the Pi are available for customisation, in a 'requirements-in/production-out' model. Upton believes that, "the first wave will be existing Rasp-

berry Pi customers." element14 and Raspberry Pi Trading's agreement to provide design and manufacturing services to OEM customers to create

bespoke designs is 'global and exclusive' based upon the Raspberry Pi technology platform.

Highly-integrated x86-architecture embedded processors from AMD

AMD's Embedded R-Series SOC processors target the embedded application markets for digital signage, retail signage, medical imaging, electronic gaming, media storage and communications and networking, with features such as advanced graphics, and extended temperature operation.

Latest generation AMD Radeon graphics, as well as the latest multimedia technology, is integrated on-chip; the AMD Embedded R-Series SOC provides enhanced GPU performance and support for High Efficiency Video Coding (HEVC) for full 4K decode and DirectX 12. R-Series parts incorporate a full HSA implementation which balances the performance

between the CPU and GPU; AMD comments that this is the first "full, 1.0" implementation of HSA (Heterogeneous System Architecture). The AMD Embedded R-Series SOC was configured for embedded use and includes features such as industrial temperature support, dual-channel DDR3 or DDR4 support with ECC (Error Correction Code), Secure Boot, and a broad range of processor options. This is, AMD says, the first implementation of DDR4 in this space. Recognising that many embedded applications will not move to DDR4 in the near future, the SoC supports use of DDR3 and a transition to DDR4.

The processors incorporate the newest AMD 64-bit x86 CPU core

High Performance ≠ High Price. Call MPS!

Premium DC/DC Power Modules

	0.6A	1A	2A	3A	6A-10A	15A	20A
36V	MPM3506A	MPM3510A	MPM3515*				
24V	MPM3606	MPM3610	MPM3620	MPM3630	MPM3680 MPM3682	MPM3684 MPM3686	
6V	MPM3805	MPM3810	MPM3820	MPM3830			
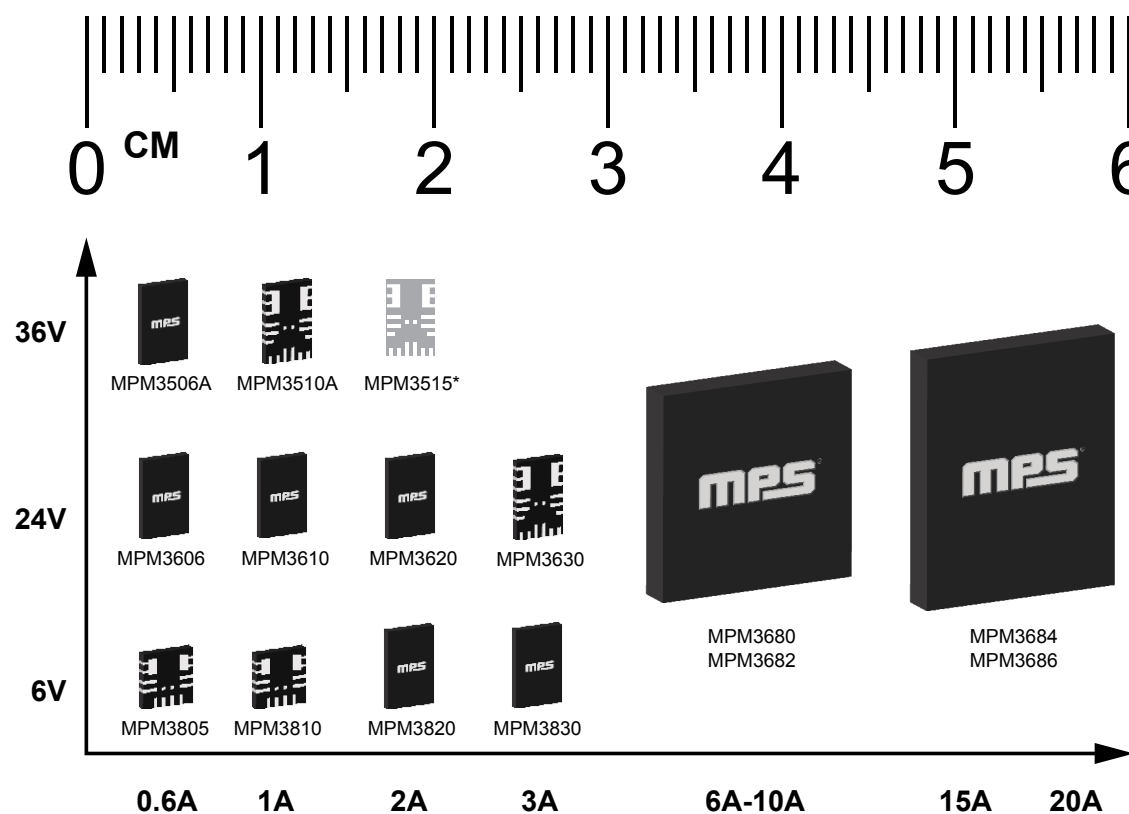
*Coming soon

Follow us on:

("Excavator"), plus third-generation Graphics Core Next GPU architecture, and advanced power management for reduced energy consumption. The single-chip system-on-chip (SOC) architecture enables simplified, small form factor board and system designs, including by third party development platform providers.

The SoC offers industrial temperature support, dual-channel DDR3 or DDR4 support with ECC (Error Correction Code), Secure Boot, and a range of processor options. Configurable thermal design power (cTDP) allows designers to adjust the TDPs from 12W to 35W in 1W increments for greater flexibility. The AMD Embedded R-Series SOC also has a 35% reduced footprint when compared to the 2nd Generation AMD Embedded R-Series APU.

AMD promises ten-year longevity of supply; processors support Windows 7, Windows Embedded 7 and 8 Standard, Windows 8.1, Windows 10, and AMD's all-open Linux driver including Mentor Embedded Linux from Mentor Graphics and their Sourcery CodeBench IDE development tools.

Complete article, here ▶

Free, pre-commercial access to ARM Cortex-M0 core

With the objective of speeding and simplifying the early stages of embedded-core SoC designs, ARM has made available free access to the IP for a pre-configured implementation of the Cortex-M0 core. This is offered via the ARM DesignStart portal, where design, simulation and prototyping can be carried out, accompanied by a low-cost, simplified licensing package for commercialisation. ARM says it is making it, "far easier to design, prototype and produce system-on-a-chip (SoC) components," by offering free pre-commercialisation use of ARM Cortex-M0 processor IP and low-cost FPGA prototyping. The package includes:

· A Cortex-M0 processor and System Design Kit (SDK), featuring system IP, peripherals, test bench and software
· A free 90 day licence for the full suite of ARM Keil MDK development tools.

The package will enable the design, simulation and testing of new SoCs using a pre-configured Cortex-M0 processor without incurring the capital costs typically associated with up-front licensing. There is an option to move to the prototyping stage with a $995 ARM Versatile Express FPGA development board.

Developers wishing to enter full commercial production can then purchase a simplified and standardised $40,000 fast track licence. This includes commercial use of ARM Cortex-M0 processor IP, SDK, and Keil MDK development tools, along with ARM technical support.

The upgraded DesignStart portal makes ARM technology available, the company asserts, to the broadest range of SoC developers, from startups to established vendors, and makes the path to full commercial production easier and faster. Click link below for the full story.
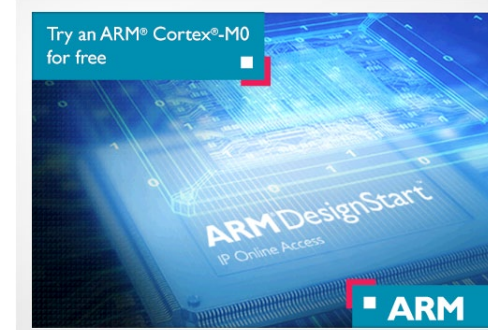
ARM buys back Carbon

In a separate move, ARM is to step up its internal development-tool support and offer cycle-accurate virtual prototyping for complex SoCs through acquisition of Carbon Design Systems; ARM has acquired the product portfolio and other business assets of Carbon. Key IP in the transaction was sold by ARM to Carbon several years ago.

This combination of assets and expertise will ARM says, enhance its capability in system-on-chip

(SoC) architectural exploration, system analysis and software bring-up. It will also enable earlier availability of cycle-accurate models for future ARM processors and ARM-based systems. The same models were developed following ARM's earlier transfer of its SoC Designer IP to Carbon.

Carbon has created a library of ARM processor and system models that can be extended to create cycle-accurate virtual prototypes of any new ARM-based SoC. The technology relies on RTL compila-tion, to ensure perfect functional and cycle accuracy. This is essential when evaluating target benchmark performance in the earliest stages of SoC design.

In future, Carbon products will be marketed as ARM Cycle Models and will remain available from ARM IP Exchange. ARM will also continue to offer Carbon's solutions for model generation and SoC analysis.

Complete article, here ▶

TI embedded SoC MCUs add real-time processing and multimedia capability

Texas Instruments' Sitara AM57x family, along with an associated processor SDK, claims new levels of integration, scalability, on-chip peripherals and ease of use. The Sitara AM57x processor family become the highest performance devices in this processor platform. Sitara AM57x processors are designed for a broad range of embedded and industrial applications through their heterogeneous architecture including ARM Cortex-A15 cores for high-performance processing and running a high-level operating system (HLOS). AM57x processors integrate TI's C66x digital signal processors (DSPs) for analytics and real-time computation, programmable real-time units (PRU) and ARM Cortex-M4 cores for control functions, and video and graphic accelerators for advanced user interfaces and multimedia applications. The device family, says TI, was designed from the ground up with high performance and integration in mind, and delivers claimed performance of more than 40% greater than quad-core ARM Cortex-A9 processors and 280% greater than standard dual-core ARM Cortex-A9 processors. Developers can choose between two different types of computing cores, both with one or two ARM Cortex-A15 cores and C66x DSPs that each perform a different task. The multicore architecture provides flexibility by distributing tasks to the right cores while driving system integration and best-in-class performance – all within one chip. AM57x processors also include two ARM Cortex-M4 cores and four PRUs (programmable real-time units) to provide low-latency, real-time control functions for industrial applications such as controlling a motor or monitoring sensors.

The processors are equipped with an industrial communica-tion subsystem (ICSS) for real-time fieldbus protocols and other industrial communication, and system flexibility with integrated high-speed peripherals such as PCIe, SATA, Gigabit Ethernet, and USB 3.0. The devices integrate one or two SGX544 3-D and a GC320 2-D graphic accelerators for advanced graphical user interfaces; a 1080p60 video accelerator and multi-display support for high-definition video playback; and multiple camera inputs for recording events, taking pictures or reading a barcode.

Complete article, here ▶

Time-of-flight IC for optical object detection/ranging within 2m

Intersil's ISL29501 signal processing IC detects objects up to two metres away; the device is a time-of-flight (ToF) signal processing IC that provides a complete object detection and distance measurement solution when combined with an external emitter (LED or laser) and photodiode. The ToF device offers ultra-small size, low-power consumption and superior performance for connected devices, as well as consumer mobile devices and the emerging commercial drone market.

The ISL29501 addresses the shortcomings of traditional amplitude-based proximity sensors and other ToF solutions that perform poorly in lighting conditions above 2,000 lux, or cannot provide distance information unless the object is perpendicular to the sensor. Alternative solutions are – Intersil asserts – too expensive, bulky or power-hungry for use in small form factor, battery-powered applications. The ISL29501 sensor provides a small solution footprint and precision long-range accuracy up to two metres in both dark and bright ambient light conditions. It allows designers to select the emitter and photodiode of their choice and configure a low power ToF sensing system customised for their application. Intersil offers a reference design featuring the ISL29501, emitter and photodiode, along with graphical user interface (GUI) software and user's guide. The ISL29501 incorporates power saving and extends battery life; an on-chip emitter DAC with programmable current up to 255 mA allows system designers to select the desired current level for driving the external infrared (IR) LED or laser. This feature enables optimisation of distance measurement, object detection and power budget. The device's single shot mode saves power by allowing designers to define the sampling period for initial object detection and approximate distance, while continuous mode more accurately measures distance. The ISL29501 also performs system calibration to accommodate performance variations of the external components across temperature and ambient light conditions. An on-chip DSP calculates ToF for accurate proximity detection and distance measurement up to two metres: modulation frequency of 4.5 MHz prevents interference with other consumer products such as IR TV remote controls that operate at 40 kHz.

"Prior to Intersil's time-of-flight technology breakthrough, there was no practical way to measure distance up to two metres in a small form factor," said Andrew Cowell, senior vice president of Mobile Power Products at Intersil.

Dialog & Bosch merge wireless & sensor expertise for gesture recognition

Dialog Semiconductor and Bosch Sensortec have announced a collaboration to develop a low power smart sensor wireless platform for IoT devices; the resulting, lowest-power 12-degrees of freedom (DOF) advanced sensor development kit can provide increased performance in gesture recognition.

The smart sensor reference platform for gesture recognition is aimed at applications in wearable computing devices and immersive gaming, including augmented reality, and 3D indoor mapping and navigation. It combines Dialog's DA14580 Bluetooth Smart

System-on-Chip (SoC) with three low power sensors from Bosch Sensortec: the BMM150 for 3-axis geo-magnetic field measurement, the BME280 pressure, humidity and temperature sensor, and the 6-axis BMI160 (a combination of a 3-axis accelerometer and 3-axis gyroscope in one chip). The resulting unit, built onto a 14 x 14 mm

printed circuit board, consumes less than 500 µA from a 3V coin cell when updating and transferring all 12 x 16 bits of data wirelessly to a smartphone.

The DA14580 SmartBond SoC is used in wearables, and integrates a Bluetooth Smart radio with an ARM Cortex-M0 application processor and intelligent power management. Bosch Sensortec's BMI160 6-axis Inertial Measurement Unit (IMU) integrates a 16 bit, 3-axis, low-g accelerometer and an ultra-low power 3-axis gyroscope within a single package.

Complete article, here ▶

Battery-based local energy storage to back renewable-energy generation

A project in southern Germany is evaluating the deployment of local energy storage to balance the generation and consumption of energy generated from solar and wind resources. Contrary to opinions that have stated that today's

battery technology is not adequate for such a task, this design uses available battery chemistries. The participating bodies are the Technical University of Munich (TUM), Kraftwerke Haag GmbH, VARTA Storage GmbH and the

Bavarian Centre for Applied Energy Research (ZAE-Bayern): who collectively observe that in many southern Germany communities roof-mounted solar panels generate more power during peak times than can be locally consumed. At other times residents must draw on electricity from trans-regional grids. Transmission losses and fluctuations in electric power grids can be reduced when renewable energy is stored locally.

With 200 kilowatt-hours of storage capacity and 250 kilowatts (peak deliverable at any time) of electrical power, the storage facility can balance the performance peaks of solar systems with the consumption peaks of connected households. It occupies a standard shipping-container outline.

The eight-ton, fully integrated storage system currently comprises
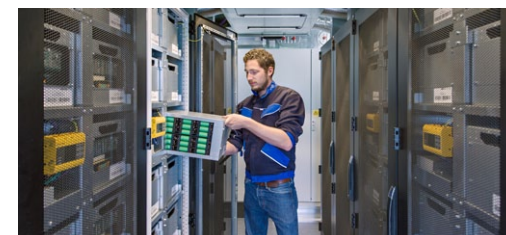
eight racks of 13 battery modules with 192 battery cells each, a battery management system and performance electronics. The EEBatt project is based around lithium-ion technologies; EEBatt uses Lithium Iron Phosphate (LFP) and Lithium Titanate Oxide (LTO) chemistry for the setup. "As required, the system can be extended in 25 kilowatt steps with further racks. With an additional transformer it can even be used as an insular, grid-independent solution," says Herbert Schein, managing director of VARTA Storage GmbH.

Complete article, here ▶

Custom programmable 9-axis motion sensor integrates ARM core

Bosch Sensortec's BMF055 is a compact 9-axis motion sensor

designed for ease of programming for a particular application. It in-

cludes accelerometer, gyroscope, magnetometer and 32 bit Cortex M0+ core in a single package: a software development package aids customisation.
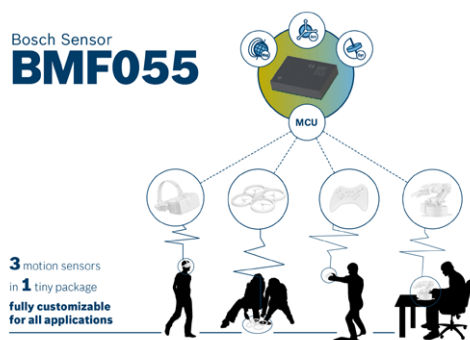
The BMF055 is aimed at designs using advanced application-specific sensor fusion algorithms, adding sophisticated motion sensing capabilities, and replacing multiple discrete components with a single package. The sensor, from Bosch Sensortec's Application-Specific Sensor Node (ASSN) fam-

ily, combines an accelerometer, a gyroscope and a magnetometer with a Cortex M0+ processor from Atmel's SAMD20 microcontroller family. In a single 5.2 x 3.8 x 1.1 mm package, it provides this high level functionality in one solution, making integration easier.

With the BMF055, Bosch Sensortec provides a Software Development Package that includes a precompiled BSX Lite fusion library with integration guidelines, API source files for individual sensors and example projects as a plugin for Atmel Studio. This software development package will enable customers to develop their own application-specific firmware for the BMF055 sensor without requiring an additional application processor.

Complete article, here ▶

sion (193i) lithography. Development of EUV technology has been a major programme at imec over several years (using light of sufficiently short wavelength to enable direct imaging of patterns at nanometre dimensions). To produce this test pattern, imec and Cadence say they optimised design rules, libraries and place-and-route technology to obtain optimal power, performance and area (PPA) scaling using Cadence's Innovus Implementation System. The geometry came from a processor design, although the exercise was – at this stage – concerned with demonstrating that patterns of the appropriate size could be defined to be laid down on silicon. In parallel with the EUV effort, imec and Cadence taped out designs using Self-Aligned Quadruple Patterning (SAQP) for 193i lithography, where metal pitches were scaled from the nominal 32nm pitch down to 24nm to push the limit of patterning.

The definition of a metal pitch of 24 nm enables what foundries may, depending on the conven-

tions they are following, choose to call "5 nm" technology. This announcement is concerned with the tape-out, that is, demonstrating that the geometric data for such a step can be generated. Vassilios Gerousis, Distinguished Engineer, Cadence and Praveen Raghavan, Principal Engineer, imec, add that, going forward, "There are three options we plan to expose: 1.) SAQP for the lines with 193i for the cuts and via (multi exposure); 2.) SAQP for the lines with EUV for the cuts and via (single exposure); and 3.) EUV for the lines and vias (no cuts needed)."

They note that there are no actual devices in the tapeout, "The objective of the tape-out is patterning, etch, lithography, metallisation, power-performance, process window and rule set learning...

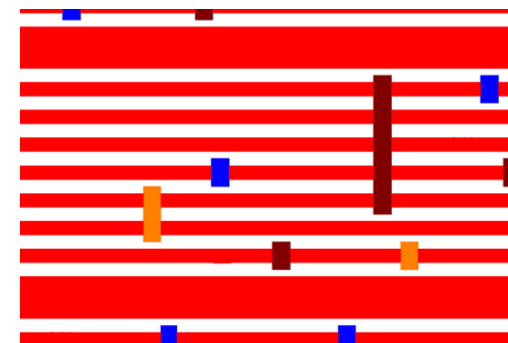# Imec & Cadence tapeout first test chip for 5-nm technologies

Nano-electronics research centre imec (Leuven, Belgium) and Cadence Design Systems,

have announced first tapeout of a 5nm test chip using extreme ultra-violet (EUV) as well as 193 immer-

the 'vehicle' is metal layers, M2-via-M3." [Metal layer 2/via/Metal layer 3.]

"However, during the place and route with Cadence's Innovus, a full processor was taken with the device model, parasitics and tim-ing closure. On the chip both the processor and SRAM were placed. The tapeout however [consists of] only M2-via-M3.

Complete article, here ▶

Not a battery, not a cap: Murata's small energy [storage] device

To meet what the company sees as a gap in the available range of energy storage solu-

tions, Murata has developed the UMAC, a small, high-capacity cylinder-type energy device for use in wearable and wireless sensor applications. Although lithium-ion based, Murata differentiates it from a battery.

The UMAC is a miniature device with a high energy storage capacity, low internal resistance, fast charging and discharging and the ability to withstand load fluctuations. It may be used as a secondary battery in the same way as a capacitor. The UMAC achieves better charge/discharge characteristics and has an extended cycle life superior to conventional batteries. Suited for use as a power supply for wearable devices or sensor nodes for wireless sensor networks, the UMAC maintains flat voltage characteristics while accommodating a wide range of load characteristics.

Designed for applications within the wearables market, the UMAC has several key safety features. Because of its small capacity and use of chemically stable materials, thermal runaway does not occur. This means that smoke or fire will not occur should a short circuit happen. The UMAC has a high rate of charge/discharge cycles and is capable of 10 cycles per hour with a maximum discharge rate of 30 mA. It also features an extended cycle life with a capacity recovery rate of 90% or higher after 1,000 cycles.

The UMAC is particularly suitable as an energy device for sensor nodes within wireless sensor networks because high-rate discharge characteristics mean that peak-assist capacitors are not required. Low self-discharge level minimises loss of stored energy and flat voltage characteristics permit use immediately after charging starts for stable device operation.

Complete article, here ▶

An IoT 'starter kit' from Arrow and Amazon Web Services

Distributor Arrow Electronics, in collaboration with Qualcomm Technologies and Amazon has disclosed its DragonBoard 410c "Internet of Things" (IoT) Starter Kit, which is based on the Qualcomm Snapdragon 410 processor and bundled with Amazon's IoT Software Development Kit (SDK). With infrastructure support by Amazon Web Services (AWS), the DragonBoard IoT Starter Kit includes the tools a developer or maker would need to start up an IoT application - in minutes, its designers claim. Amazon selected Arrow to support its new SDK and provide IoT products with AWS support to the developer community. Arrow, which has a dedicated effort in IoT adoption, says that it, "Wanted to provide developers and makers with a low-cost, high-performance way to build IoT

solutions."

The DragonBoard IoT Starter Kit is based on the DragonBoard 410c (pictured), a low-cost, high-performance Arrow-built development board that features the 64-bit capable Snapdragon 410 quad-core ARM Cortex A53 processor. Based on Linaro's open-source 96Boards specification, the DragonBoard offers advanced processing power, WLAN, Bluetooth, and GPS – in a board the size of a credit card.

Complete article, here ▶

Electrometer-grade amp for highest-sensitivity measurements

Aimed at applications such as chemical analysis instruments, and in other pico-amp-level detection circuits, Analog Devices has introduced an electrometer-grade operational amplifier that yields the highest level of precision and data repeatability over a wider temperature range.

The ADA4530-1 op amp's input bias current is 250 fA at 125°C, which ADI says is 20 times lower than competitive amplifiers, and drops to 20 fA at 85°C, which is 50 times lower than compet-

ing devices. It is the only op amp able to specify the same input bias current of 20 fA from room temperature to 85°C and is the only amp in its class to be fully production tested for bias current at room temperature and 125°C. The closest competing op amps – ADI asserts – are rarely specified at 125°C and none are production tested at room temperature for the bias current, which prevents system designers from taking full advantage of the sensitivity of their sensors, because they need

to leave some guard band for a wider variation of the bias current. It operates from ±2.5 to ±8V, or 5 to 16V: its low bias current makes the ADA4530-1 suitable for interfacing to sensors that are sensitive to output loading such as photo diodes and other high output impedance sensors often used in precision monitoring/analysis equipment such as spectrophotometers, chromatographs and mass spectrometers, as well

as potentiostatic and amperostatic coulometry measurement devices. The new amp also can be used as a front-end amplifier for picoammeter and coulomb-meter instrumentation systems, as a transimpedance amplifier for photodiodes, ion chambers, and working electrode measurements, or as a high-impedance buffer for chemical and capacitive sensors.

Complete article, here ▶

Arduino-compatible, ARM mbed MCU development platform, from Maxim

Maxim Integrated has posted details of a development platform for its own ARM-based MAX32600 microcontroller; it offers an ultra-low-power ARM Cortex-M3 with advanced analogue front-end in an Arduino-compatible form factor. The MAX-32600MBED provides a platform for evaluating the capabilities of the MAX32600 microcontroller. The MAX32600MBED also provides a complete, functional

system ideal for developing and debugging applications.

The board includes a MAX32600 Cortex-M3 microcontroller, prototyping area with adjacent access to precision analogue front end (AFE) connections, I/O access through Arduino-compatible connectors, additional I/O access through 100mil x 100mil (0.1 x 0.1 in., 2.54 x 2.54 mm) headers, USB interface, and other general-purpose I/O devices.
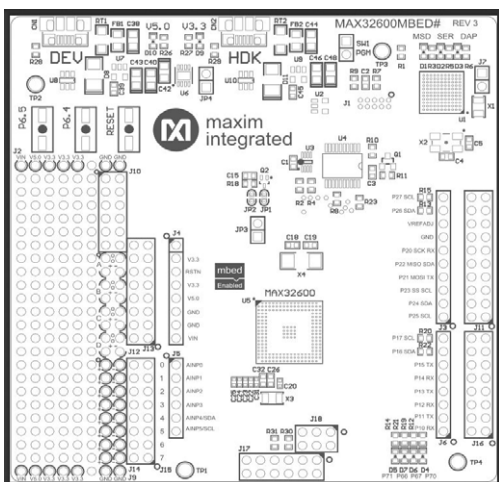
An on-Board ARM mbed Hardware Development Kit (HDK) interface provides quick connection to toolchains; Arduino-compatible connectors provide connectivity to existing component boards; and Serial Peripheral Interface (SPI) and Inter-Integrated Circuit (I²C) connectivity on a 2 x 6 header provide connectivity to existing evaluation modules.

Complete article, here

2.3 Mpixel automotive image sensor carries ASIL B qualification

ON Semiconductor is sampling its next generation ADAS (advanced driver assistance systems) automotive image sensor with LED Flicker Mitigation and ASIL B support.

ON Semi is seeing a marked increase in the number of image sensors deployed per car in ADAS functions. Its most recent introduction provides, among other features, flicker reduction. This is intended to eliminate, directly at the sensor, the strobing effect that

can occur when the image sampling cycle 'beats' with the pulsed waveform driving LED tail-lights in other vehicles, or illuminated speed-limit signs.

The sensor also has a high dynamic range, substantially exceeding that of the human eye; and it is also the only sensor in its applications space, ON claims, to have ASIL B support. Using a 4-exposure capture cycle to achieve HDR (high dynamic range) the device can reach frame rates

of up to 40 fps, and dynamic range of 120 dB.

The LED Flicker Mitigation (LFM) technology in the sensor eliminates high frequency LED flicker from traffic signs and vehicle LED lighting and allows Traffic Sign Reading algorithms to operate in all light conditions. The AR0231AT has a 1 / 2.7 in. (6.82 mm) optical format and a 1928 (horizontal) x 1208 (vertical) active pixel array. It uses 3.0 micron Back Side Illuminated (BSI) pixels with ON Semiconductor's DR-Pix technology, which offers dual conversion gain for improved performance under all lighting conditions. It captures images in linear, HDR or LFM modes, and offers frame-to-frame context switching between modes and has multiple data interfaces including MIPI,

parallel and HiSPi. Other features include selectable automatic or user controlled black level control, spread-spectrum input clock support and multiple colour filter array options.

AR0231AT occupies an 11 x 10 mm iBGA-121 package and engineering samples are available now. It has an operating temperature range of -40 to +105C (ambient) and will be fully AEC-Q100 qualified. It will be available in mass production in 2016.

Complete article, here

VIDEO SECURITY SYSTEMS BENEFIT FROM HIGH VOLTAGE FLYBACK CONTROLLERS

By Bruce Haug, Linear Technology

In order to get complete surveillance coverage for many installations, Installations of several hundred cameras may be necessary. Surveillance cameras typically operate from a 24V DC or 12V DC supply voltage at power levels up to 25W. However, the 12V or 24V input is not normally available in most cases and needs to be developed. Most installations have an AC mains voltage available such as 220VAC (180-265VAC), or 110VAC nominal (90-132VAC). Operating from AC mains also requires isolation from input to output for safety purposes.

Flyback converters have been widely used in isolated DC/DC applications for many years, but are not necessarily a designer's first choice. Power supply designers may choose a flyback out of necessity for lower power isolated requirements, not because they are easier to design. Flyback converters have stability issues due to the well-known right-half-plane zero in the control loop that is further complicated by the propagation delay, ageing and gain variation of an optocoupler. Furthermore, a flyback converter requires a significant amount of time devoted to the design of the transformer, a task further complicated by the – normally limited – selection of off-the-shelf transformers and the possible necessity for a custom transformer. So how can the power supply designer get help?

Primary-side sensing IC simplifies design

A recently-introduced isolated flyback controller resolves many of these flyback converter design challenges. First of all, the LT3798 eliminates the need for an optocoupler, secondary-side reference voltage and extra third winding off the power transformer, all while maintaining isolation between the primary- and secondary-side with only one part required to cross the isolation barrier. In addition, the device incorporates active power factor correction (PFC) into the converter. This feature also allows the controller to provide a single stage converter that provides an isolated flyback and active PFC into a single converter.

The IC employs a primary-side sensing scheme that is capable of detecting the output voltage through the flyback primary-side switching node waveform. During the switch off-period, the output diode delivers the current to the output, and the output voltage is reflected to the primary-side of the flyback transformer. The magnitude of the switch node
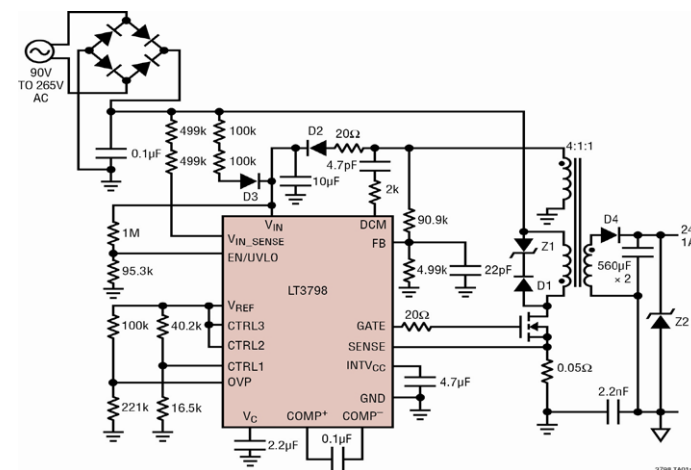

Figure 1. *Flyback converter with primary-side output voltage sensing*

voltage is the summation of the input voltage and reflected output voltage, which the LT3798 is able to reconstruct. This output voltage feedback technique results in better than ±5% total regulation over the full line voltage input, temperature range and load range. Figure 1 shows a flyback converter schematic.

The article continues by expanding on the mechanism used to ensure effective load regulation from the primary side of the converter, and provides more practical parts-list suggestions. Click for pdf.

Download PDF of Article

Find high voltage flyback controllers on EETsearch

POWER SUPPLIES

A MULTIPLE-OUTPUT PRIMARY-SIDE REGULATED QUASI-RESONANT FLYBACK POWER SUPPLY

By Florian Mueller, Texas Instruments

This article presents a primary-side regulated quasi-resonant flyback with multiple outputs. A primary side regulated flyback configuration does not need an optical coupler. It uses magnetic feedback via the main transformer's bias winding to close the feedback loop.

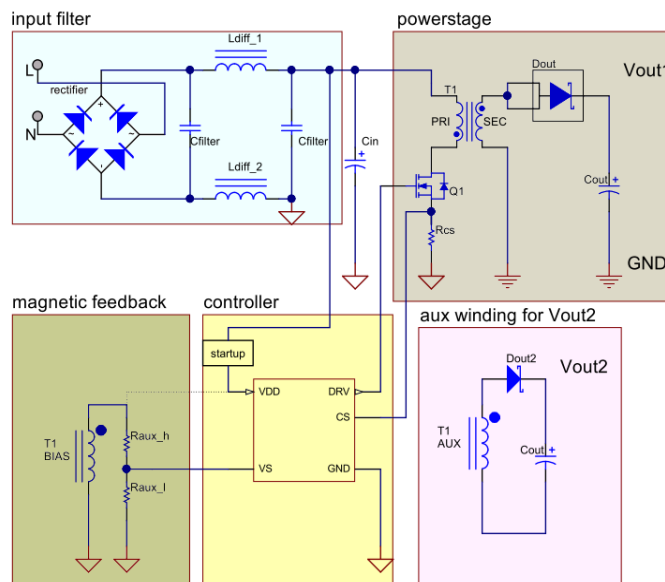The winding used to provide that feedback is needed (otherwise) to provide the supply voltage for the controller, and a simple resistor divider (Figure 1: Raux-h, Raux_l) is sufficient to obtain the information for regulating the output voltage. Therefore, the primary side regulated flyback is one of the cheapest isolated offline topologies.

A good example of this is the reference design PMP10168 from the Texas Instruments power reference design team. The PMP10168 uses a primary side regulated quasi-resonant (QR) flyback controller to generate two isolated outputs from an AC input source.

V_{out} = output voltage
V_F = forward voltage of the output diode
$I_s \times R_s$ = resistance voltage drop due to secondary current
N_A = number of transformer bias windings
N_P = number of transformer primary windings
N_S = number of transformer secondary windings
V_{BLK} = input bulk voltage

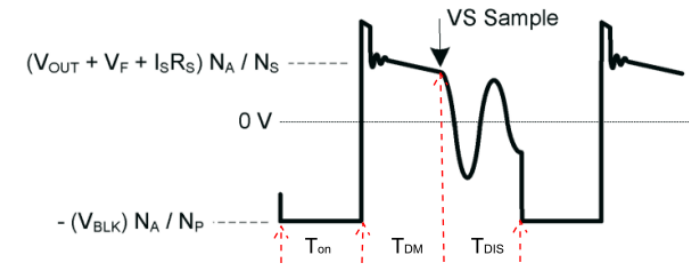**Figure 1.** *Primary side regulation principles*

Figure 2. *Bias winding voltage*

The bias winding (Figure 1: T1 BIAS) is connected in phase with the output winding and has four main purposes. It delivers the power for the controller; it measures the input voltage during the on-time of the primary FET Q1; it senses the demagnetisation time of the transformer in order to ensure Discontinuous Conduction Mode (DCM) operation; and it delivers information to regulate the output voltage.

How does it work? The author demonstrates with, firstly, consideration of the voltage waveform on the bias winding... click for pdf.

Download PDF of Article

Find flyback power supply on EETsearch

INDUSTRIAL ETHERNET INTERFACE 4.0

By Volker Goller, Innovasic

What is required from the next generation of industrial Ethernet interfaces: A look at the standard protocols that exist today and where they are headed

In the beginning there was fieldbus

When the first fieldbuses emerged from the mid to late 1980s (who can now remember BITBUS, 1N/Seab or PNET?) it quickly became clear that fieldbuses would be a success story. The quality of the technologies at the time is demonstrated by the fact that important systems around the world continue to successfully operate these initial fieldbuses today.

Then, during the initial deliberations on replacing fieldbuses with a network technology based on Ethernet, the hope arose – for a time – that the industry would be able to agree on a standard protocol. As history shows, this hope was in vain. Today, there are almost as many industrial Ethernet protocols as there were fieldbuses. Some say that there are even more. Fortunately, to date, only a few have proven to be relevant for the market. These primarily include PROFINET, EtherNet/IP, EtherCat, Sercos III and Powerlink.

Although all these protocols have to solve the same basic problems, some use completely different concepts to do so. Technology modules in the form of integrated circuits and optimised microcontrollers are required to implement these protocols. And, on top of that, the protocol software also has to be aligned to the industrial application.

Challenge of Industrial Ethernet

The challenges of developing efficient solutions for the industrial use of Ethernet are manifold.

The first is real-time capability: Depending on the protocol and application, cycle times of below 31.25 µsec are possible. A number of modifications to the hardware and the Ethernet protocol itself are necessary for this to be achieved using 100 MBit/sec Ethernet, which is used by the overwhelming number of industrial Ethernet protocols. Moreover, the requirements for the consistent quality of the cycle times are extremely high. Fluctuations in the cycle time, referred to as jitter, must be minimised. This cannot be realised effectively without prioritising communication.

A look at the software architecture shows that this also has special requirements in order to ensure the high real-time performance of the application. Traditional operating systems are established in horizontal layers. But the application tends to require more vertical access to the real-time data. The absence of this kind of architecture leads to jitter due to task changes and interprocess communication at each of the horizontal layers.

Innovasic's PriorityChannel technology has been conceived to address precisely these two points; prioritisation and software architecture. Current field devices have shown that they perform extremely well in the ODVA LoadTest as well as the PI SecurityTester Level 1 using PriorityChannel, which is reflected in CLASS III certification by SecurityTester Level1 (CLASS III is currently the highest defined performance class by SecurityTester). In particular, it is the interaction between appropriate prioritisation in hardware and software as well as the selection of appropriate software architecture that enables this performance.

The article continues by looking at auxiliary protocols; switch configurations in industrial Ethernet; and protocol evolution. Click for pdf.

Download PDF of Article

Find Industrial Ethernet Interface 4.0 on EETsearch

EMBEDDED SECURITY

GUIDELINES FOR BUILDING A SECURE DEVICE

By André Schmitz and Rolland Dudemaine, Green Hills Software

Security cannot be an afterthought. As security breaches become more and more publicised, it is also apparent that even industrial devices – not meant to be actively driving security in the enterprise network – must be secured. Application architects need to carefully think through the interactions between software and hardware components and the resultant behaviour in order to make a Secure Device resilient to well known, and less common, misuses.

This article covers some of the principles necessary to build a Secure Device, looking at the boot process, system-level considerations about time and space partitioning, and OS choice. It discusses some application-level design patterns which help improve the security and safety of devices in a systematic way.

Definitions

From a general perspective you can define security as a condition of protection from hostile acts through protective measures. In the area of computer science this definition can be made much more specific. There is a definition of "security" in the National Information Systems Security Glossary which says that security provides "Protection of information systems against unauthorised access to, or modification of, information, whether in storage, processing or transit, and against the denial of service to authorised users, including those measures necessary to detect, document, and counter such threats" [Reference 1].

Security in electronic devices is needed for different purposes, which can be distinguished depending on the type of information to be secured or the people affected by its absence. Everyone is certainly interested in the protection of his or her privacy, including the protection of medical information or other personal data. When it comes to the economic consequences of being insecure people would like to see their credit card or bank account information secured and want to use secure automatic teller machines. The community in general is interested in national security and the reliability of public services.

Results of the absence of security are known to everyone. There are spyware attacks and viruses on Personal Computers and thousands of websites get hacked daily. At first sight it may look as if security is a topic only needed on desktop computing, but this is not true. There have been several security breaches into embedded systems in the past and Table 1 lists a few examples.

Year	Security Breach
2000	Gazprom gas pipeline control system overtaken
2005	Greek Ministry of Defence phones wire tapped [2]
2007	Insider hack of Los Angeles traffic light system [3]
2008	Hackers shut down power grids in several regions [4]
2011	Counterfeit RSA Tokens affect several big companies
2014	Sony Pictures Entertainment hack
2015	Security researchers hack Chrysler's dashboard PCs

Table 1. *Examples of security breaches in embedded systems*

Certification of security

When providing secure software, it might be necessary to evaluate how secure the software actually is and whether it is more or less secure compared to another piece of software. For that purpose the Common Criteria for Information Technology Security Evaluation (ISO/IEC 15408, abbreviated as Common Criteria or CC) was implemented, an international standard for evaluation of security in IT products. The purpose of the Common Criteria is to develop standard packages of commonly found requirements (a.k.a. Protection Profiles, or PP) and to have a standard process of independent evaluation by which an expert evaluation team arrives at a level of assurance for some particular product (Evaluation Assurance Level, or EAL). As a customer, this makes your life simpler, because you can compare your needs against existing requirements constructed by experts

and see how well the software meets your requirements.

All certifications are coded as a pair of <PP>/<EAL> for a defined product. The Protection Profile tells you how good the protection is under what conditions. That means, it provides an implementation independent specification of information assurance security requirements. It is a combination of threats, security objectives, assumptions, security functional requirements (SFRs), security assurance requirements (SARs) and rationales [5]. Note that virtually everybody can write his own Protection Profile, and this is what companies tend to do. Unfortunately those Protection Profiles tend to be too specific to a single product which makes them hardly usable for other products. The Evaluation Assurance Level specifies how sure you are that the target of evaluation (TOE) actually provides the protection advertised in the PP. It is a combination of requirements for analysis of a secure product in a format defined by Common Criteria.

The highest certification ever done for an Operation System is SKPP/EAL6+ [6], where SKPP stands for the Separation Kernel Protection Profile, a security requirements specification for separation kernels suitable to be used in the most hostile threat environments. The SKPP was published by the Information Assurance Directorate of the U.S. National Security Agency (NSA).

Even if you do not need to certify your own product, you can certainly benefit from elements that have gone through that effort already. The following sections shows how to increase security of your device.

How to make a system secure

There are numerous requirements for a secure software system. Some of them depend on the application itself and some of them are somewhat generic. The following list of requirements are rather generic and apply to all software systems:
- Provide fast and secure system start-up and boot to make sure the trusted application is running unmodified
- Allow safe and secure communication between components
- Guarantee time availability to all safety critical tasks to prevent denial of service
- Detect intrusion into the system
- Detect crash
- Allow detection and recovery for the above

An architecture that has a high requirement on security is the "Multiple Independent Levels of Security" architecture (abbreviated to MILS). It is a high-assurance security architecture based on the concepts of separation and controlled information flow. John Rushby proposed a Separation Kernel as a solution to provide multilevel secure operation on general-purpose multi-user systems [7]. A Separation Kernel is a type of security kernel used to simulate a distributed environment in a way that each regime must appear as a separate, isolated machine and that information can only flow from one machine to another along known external communication lines.

The MILS architecture requires security policies for the underlying Separation Kernel which are [8]

Information Flow : only authenticated elements communicate
Data Isolation : private data remains private
Periods Processing : no time covert channel
Damage Limitation : failure detection and handling

This is a reasonable approach to define system security in general, which can be applied to any application. *The authors continue with discussion of secure boot, secure system architecture, applications development, and integration of legacy code; click for pdf.*

Download PDF of Article

Find Embedded security on EETsearch

ADC NOISE SPECTRAL DENSITY   BY IAN BEAVERS, ANALOG DEVICES

Over time, the high speed analogue to digital converter (ADC) performance metric that mattered most has changed. As a result of signal acquisition systems' insatiable bandwidth requirements, the way in which ADCs are measured on performance has also changed. Noise Spectral Density (NSD) is another comprehensive specification used to define ADC performance.

NSD defines the entire noise power, per unit of bandwidth, sampled at an ADC input. For a Nyquist-rate ADC, noise is spread across the entire Nyquist band (Fs/2). They are "equal opportunity" noise receivers across the Nyquist. The term dBFS/Hz means that noise is defined in units of power (dB) relative to the ADC full scale within frequency bin widths of one Hertz. NSD may also be defined by dBm/Hz.

Contrast this with an FFT bin size defined as the Nyquist divided by FFT samples, with units of frequency. Regardless of the
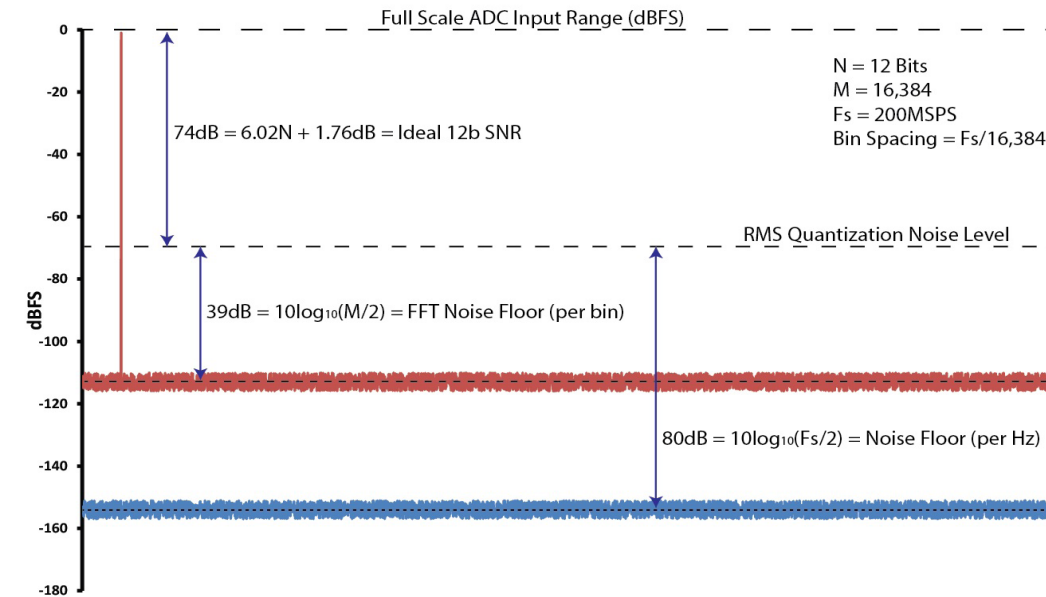

Figure 1. *A Nyquist ADC's quantisation and FFT noise floor across a Nyquist zone are compared to its NSD. FFT noise per bin is determined by the number of samples, while NSD is defined with a 1-Hz bin width.*

FFT bin frequency size, total noise is not changing. It is still spread across the same Nyquist spectrum.

SNR is the log ratio of signal power to total non-signal power. There are several non-signal power components, such as quantisation noise, thermal noise, and small errors within the ADC design. The ADC nonlinearly converts continuous signals into discrete levels. Quantisation noise is inherently created, being the difference between the analogue input and the smallest discrete least significant bit (LSB). A Nyquist-Rate ADC sampling at 2x the

frequency, spreads flat quantisation noise from DC to the Nyquist frequency wider and lower by 3dB across twice the bandwidth. Noise Power = $10\log_{10}(Fs/2)$.

For an ideal ADC, the quantisation noise limited SNR equals 6.02*N +1.76 dB. By subtracting signal power from ADC full scale power, the remainder is total noise power. Summing the 1 Hz bins of noise yields a single power noise number equal to the ADC full scale, less the signal.

To find NSD, the noise must be subtracted from the full scale signal power.

If an ideal 12-bit 200 Msample/sec ADC has SNR = 74.04 dB, its noise is spread across a 100 MHz Nyquist.

Noise Power per 1 Hz bin = $-10\log_{10}(Fs/2)$ = -80 dBFS/Hz and NSD would be -154.04 dBFS/Hz. A state of the art 12-bit 1 Gsample/sec ADC, AD9234, provides NSD of -151 dBFS/Hz.

EMBEDDED SOFTWARE

5 TIPS FOR DESIGNING INTERFACES TO REUSABLE SOFTWARE MODULES

BY JACOB BENINGO

Creating consistent and proper interfaces for reusable software modules is one of the most critical and overlooked aspects of embedded software design. Interfaces are usually developed on the fly with little to no forethought. But in order to ensure that software can easily be used from one application to the next, there are five tips that every developer should keep in mind.

Tip #1 – Start with a list of required operations

Before ever beginning to write an interface for a software module, a developer should take a few moments to write out a simple list of operations that the interface needs to perform. The list acts as a scratch pad for a developer to think through what exactly the interface needs to be doing. What are the module's operations? What are the inputs it needs? What are the outputs it will produce? All three of these questions need to be answered. The list and the questions will serve as the starting point for designing the interface.

Tip #2 – Use a UML Class Diagram

A UML class diagram is used to represent a class but it can also be used to represent a module and, more importantly, the module interface. The basic component of a class diagram is a box consisting of three sections. The first section (the top) contains the module's name. The second section (the middle) contains the module's attributes. The third and final section is used to define the operations and methods that the interface publicly exposes.

The module's attributes can be thought of as both the private and public variables that the operation of the interface will manipulate. A plus sign in front of the attribute indicates that it is public and exposed directly as part of the interface. A minus sign indicates that the attribute is private and only manipulated behind the scenes through the use of operations that the interface exposes. Think of these operations as the same ones that were listed as part of Tip #1. Figure 1 shows an example of a generic module definition on the left and a streamlined interface for an EEPROM module.

Tip #3 – Separate the interface from the implementation

When beginning to develop an interface to a module, a developer should do everything that they can to separate the interface from the module's implementation. The details of the interface's public facing portions should all be contained in the header file, which in this case defines the module's interface. The implemen-
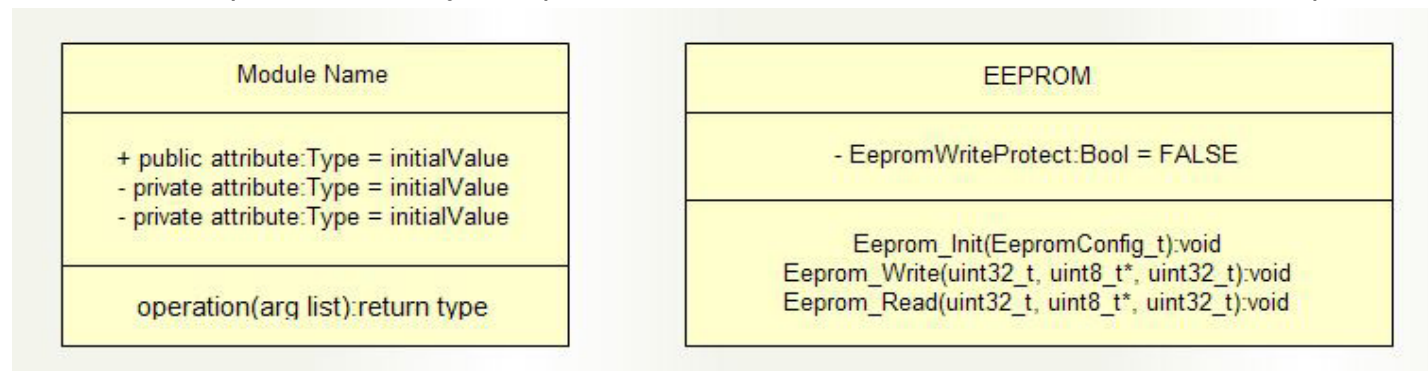

Figure 1. *Example Class / Module Diagram*

tation details should be kept in the source file. Keeping the details of implementation separate from the interface begins to provide a developer with the ability to hide the implementation. This hiding results in an abstraction of the module's class and provides the capability to later redefine the implementation without affecting the interface.

Tip #4 – Use abstract data types

Requirements always change and anticipating how requirements are going to change is usually a futile activity, even if one is equipped with a crystal ball. Abstract data types are meant to help developers deal with changing requirements. Take for example a data structure defined as part of the interface, in the header file. Any module that references the header file has the ability to create and modify data based on that data structure. When requirements change and that data structure is changed, the result is a need to provide updates to any file that used the header file. Had the developer instead created an abstract data type, one in which the details of the data structure were hidden in the implementation, only the source file implementation would need to be updated. Any modules that used the header file would simply continue to use the public interface and the underlying implementation would deal with the changed data type.

Tip #5 – Encapsulate the data

One of the first concepts taught in computer science courses is that a variable or object should be limited to the smallest program scope possible. Similarly, details of how an interface is implemented should be limited to a need-to-know basis. Developers should attempt to hide as much data and implementation as possible from the module's users. Hiding the details can help prevent users from directly manipulating a module's internal data, which could then cause the module to enter into an unknown or inconsistent state.

Final thoughts

Development is fraught with changing requirements and short development cycles. Using proper interface design techniques can improve software's overall design and minimise the impact of the ever- elusive moving target of requirements. We've examined five simple tips for designing an interface. What other considerations should developers keep in mind when developing an interface that will stand the test of time?

Jacob Beningo is a Certified Software Development Professional (CSDP) whose expertise is in embedded software. Feel free to contact him at jacob@beningo.com, and at his website www.beningo.com

USB 3.1 TESTING, PART 3: POWER DELIVERY

By Randy White, Tektronix

Read part 1 of this series on the basics of transmitter and receiver testing for the latest version of USB; and part 2 on type-C cable assemblies.

The USB PD (Power Delivery) revision 2.0 is the perfect complement to the new USB 3.1 Type-C connector. Just as the Type-C connector is fully reversible and could eventually be used on virtually every device you can and can't imagine. PD will make sure power flows bi-directionally across devices—from laptops to displays—based on which device has power to spare and which needs power. Add in DisplayPort capabilities via Alternate Mode, and you have the interconnect people have wanted for years.

As with all previous USB iterations, you expect to simply plug in your device and everything will "just work". Getting to the "just works" phase for something as ambitious as USB Type-C, however, implies that products will need extensive and thorough interoperability testing under a comprehensive range of scenarios and conditions. In the case of PD, this presents a significant challenge caused by the large number of conditions that must be tested
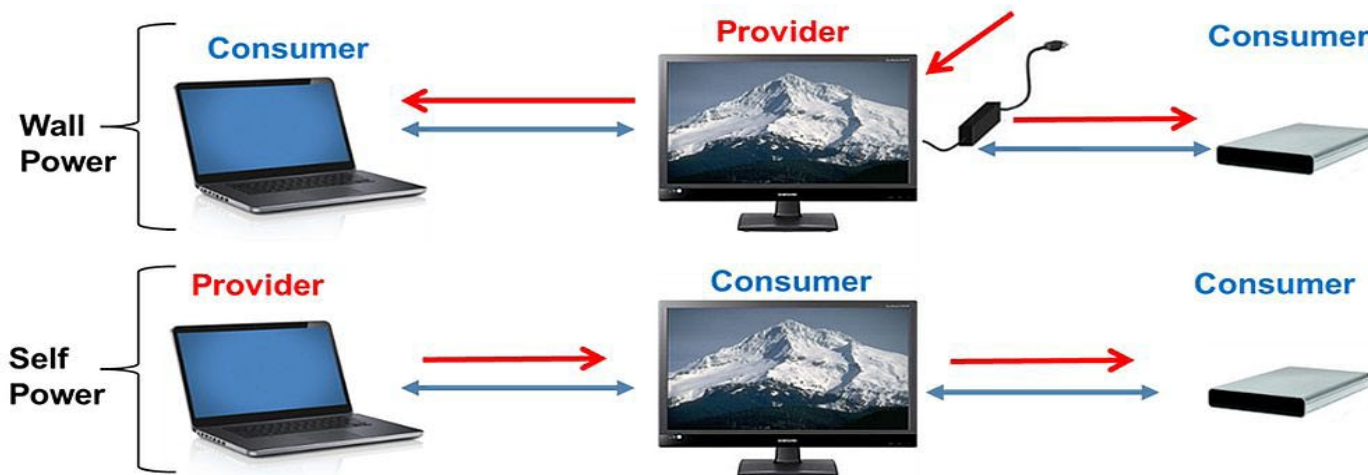

Figure 1. *The Power Delivery Rev 2.0 specification is intended to improve power handling and improve the user experience for multi-device setups.*

and, currently, the lack of formal compliance test requirements and certification programs.

The original USB Power Delivery specification dates back to July 2012 for use on standard type A and B connections to deliver increased power. This specification defined five fixed-power profiles for the power sources and mapped out a flexible power management scheme that let devices request power at an appropriate level through a bidirectional data channel. The power configuration protocol

used a 24 MHz BFSK (binary frequency-shift-keying)-coded transmission channel on the V_{BUS} line.

A new version of the power delivery specification was released in August 2014 as part of the USB 3.1 suite and has been updated slightly since then. The current specification is Power Delivery Rev. 2.0, Version 1.1 and was released in May 2015. It covers the Type-C cable with four power/ground pairs and a separate configuration channel (CC), which now hosts a DC

coupled low-frequency BMC (Biphase Mark Code)-coded data channel that is intended to help reduce RF interference. PD protocols were also updated to facilitate such Type-C features as cable ID function, Alternate Mode negotiation, increased V_{BUS} currents, and V_{CONN}-powered accessories.

The updates work to improve power handling and make the user experience better with multi device setups such as what's shown in Figure 1. In addition to the providing up to 100W (which requires a higher V_{BUS} voltage) the direction of the power sourcing can be dynamically configured, which is referred to as a role swap. The additional control signals provided with the Type-C connector will make this operation slightly easier than trying to fit this into the legacy connectors. As you can imagine, the example configurations similar to what's shown with the two setups in Fig. 1 require additional protocol support. One of the more challenging parts of testing PD is checking the protocol and operational states that can vary significantly in this environment.

Adding to the challenges of PD testing—beyond the 500-page specification itself—is the overlap across the various USB 3.1 testing programs including USB 3.1 Tx/Rx, Type-C testing, alt-mode testing and more (Figure 2). There are also issues around the reversible Type-C cable, which adds another "wrinkle" that validation

engineers will need to handle. When a connector is turned or reversed, the Tx/Rx pairs are actually re-routed to a different pair. This means that tests will need to happen with the connector in one direction, and then again with the connector reversed—a time consuming process. In some cases such as USB 3.1 Gen2 (10 Gb/sec), Dual-Role Device supporting Gen1 (5 Gb/sec) backwards compatibility as well as Sink/Source capabilities means the test coverage multiplies exponentially.

The article continues with a description of the test setup, and considers interoperability testing; click for pdf.
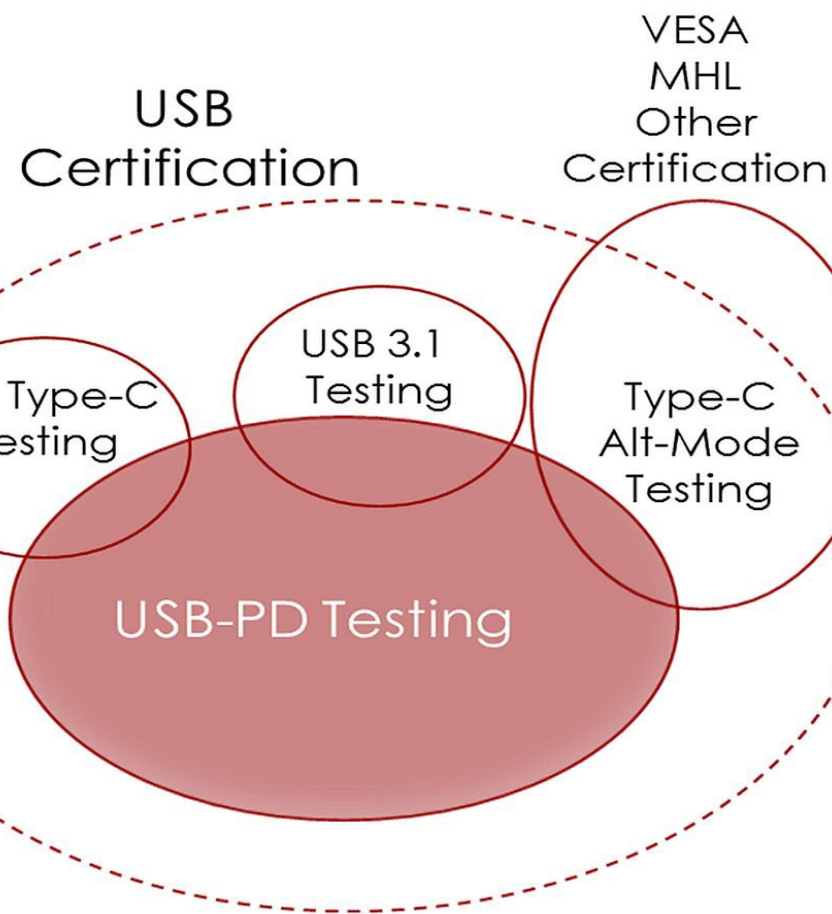

Figure 2. *USB Power Delivery testing involves more than just testing to ensure compliance with the 500-page specification due to overlap with other USB 3.1 testing as well as alt-mode.*

Download PDF of Article

Find USB 3.1 testing on EETsearch

designideas

- **Programmable-gain amp achieves high gains**
- **Avago Tech Note: Strain sensing using optical phase interrogation technique with polymer optical fibre**

Programmable-gain amp achieves high gains   By Carlos Castro-Miguens

Most data acquisition systems with a wide dynamic range need some method of adjusting the input signal level to the analogue-to-digital converter (ADC) to maximise use of the ADC's full-scale input voltage range. To achieve this, a programmable-gain amplifier (PGA) or a variable-gain amplifier (VGA) is usually located between a sensor and its ADC, as shown in Figure 1. Additional signal conditioning may take place before or after the PGA or VGA, depending on the application.
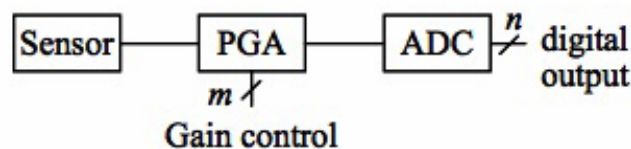

Figure 1. *PGA in data acquisition system*

When high gains are needed, the topology of the PGA circuit deserves extra thought. It is not advisable to use feedback resistors with a very high value (>1 MΩ) due to noise and op-amp offset current. In addition, for an inverting amp, high gain can result in low input resistance. This Design Idea presents a PGA circuit which

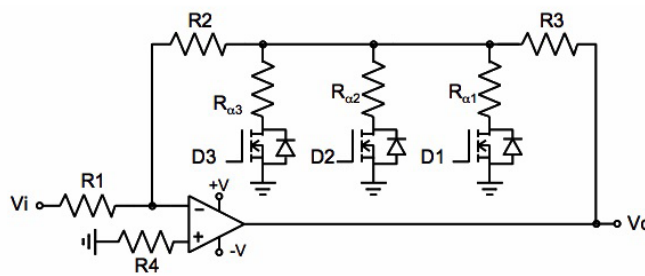satisfies these conditions. Figure 2 shows the two versions, having eight digitally programmable gains.

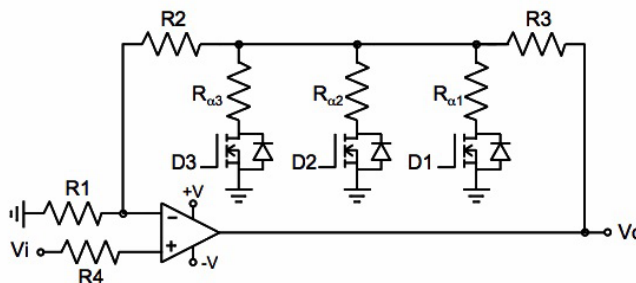**Figure 2a.** *Inverting PGA circuit*

Figure 2b. *Non-inverting PGA circuit*

Although the number of gains that can be implemented with these circuits is equal to 2^n, where n is the number of MOSFETs used, it is only possible to implement n+1 *independent* gains.

Signals D_1, D_2, and D_3 select the gain of the amplifier. The switches will typically be "logic level" MOSFETs with R_{DSon} as low as possible (e.g., 2N7002P with R_{DSon} (typ) = 1Ω or IRLML2502 with a R_{DSon} (typ) = 0.05Ω).
The independent gains that can be selected in the amplifier circuit shown in Figure 2a are:

$$D_3\,D_2\,D_1 = 0\,0\,0 \quad \rightarrow \quad G_0 = \frac{v_0}{v_i} = \frac{-1}{R_1}\left[R_2 + R_3\right]$$

$$D_3\,D_2\,D_1 = 0\,0\,1 \quad \rightarrow \quad G_1 = \frac{v_0}{v_i} = \frac{-1}{R_1}\left[R_2 + R_3 + \frac{R_2 R_3}{R_{\alpha1}}\right]$$

$$D_3\,D_2\,D_1 = 0\,1\,0 \quad \rightarrow \quad G_2 = \frac{v_0}{v_i} = \frac{-1}{R_1}\left[R_2 + R_3 + \frac{R_2 R_3}{R_{\alpha2}}\right]$$

$$D_3\,D_2\,D_1 = 1\,0\,0 \quad \rightarrow \quad G_3 = \frac{v_0}{v_i} = \frac{-1}{R_1}\left[R_2 + R_3 + \frac{R_2 R_3}{R_{\alpha3}}\right]$$

Restrictions
For Figure 2a, when two or more MOSFETs are used, the MOSFET body diodes will start to conduct if the input voltage (v_i) takes too large a value, distorting the output voltage of the amplifier. To avoid this, the following condition must be satisfied:

$$v_i \leq \frac{R_1}{R_2} \cdot v_F$$

where vF is the body diode forward voltage of the MOSFET ($v_F > 0$).

When only one MOSFET is used, the input voltage must fulfil the following condition to avoid body diode conduction:

$$v_i \leq \frac{R_1}{R_2}\left(1 + \frac{R_\alpha}{R_{DS\,on}}\right) \cdot v_F$$

The independent gains that can be selected in the amplifier circuit shown in Figure 2b are:

$$D_3\,D_2\,D_1 = 0\,0\,0 \;\rightarrow\; G_0 = \frac{v_0}{v_i} = \frac{R_1 + R_2 + R_3}{R_1}$$

$$D_3\,D_2\,D_1 = 0\,0\,1 \;\rightarrow\; G_1 = \frac{v_0}{v_i} = \frac{R_3}{R_1}\left[1 + \frac{R_1 + R_2}{R_3 P R_{\alpha 1}}\right]$$

$$D_3\,D_2\,D_1 = 0\,1\,0 \;\rightarrow\; G_2 = \frac{v_0}{v_i} = \frac{R_3}{R_1}\left[1 + \frac{R_1 + R_2}{R_3 P R_{\alpha 2}}\right]$$

$$D_3\,D_2\,D_1 = 1\,0\,0 \;\rightarrow\; G_3 = \frac{v_0}{v_i} = \frac{R_3}{R_1}\left[1 + \frac{R_1 + R_2}{R_3 P R_{\alpha 3}}\right]$$

For Figure 2b, when using two or more MOSFETs, the body diodes will conduct if the input voltage (v_i) takes too large a negative value. To avoid this, the following condition must be satisfied:

$$v_i \geq \frac{-v_F}{1 + R_2/R_1}$$

When only one MOSFET is used, the input voltage must fulfill the following condition to avoid body diode conduction:

$$v_i \geq -\left(\frac{1 + R_\alpha/R_{DS-on}}{1 + R_2/R_1}\right) \cdot v_F$$

Figure 3 shows a practical application of the circuit of Figure 2a. In this example, a PGA is used to amplify the output voltage (v_i) of a circuit that integrates and filters the signal generated by a Rogowski coil.
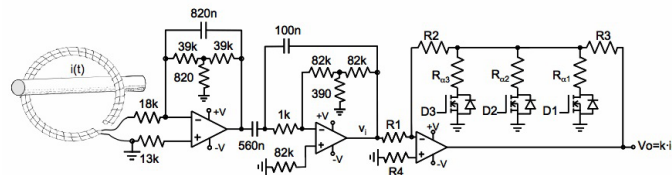

Figure 3. *AC measurement system based on a Rogowski coil*

It has been assumed that the ADC that will sample the signal $v_o = k \cdot i(t)$ has reference voltages of $v_{ref}+ = 2.5u/c$ V and $v_{ref}- = -2.5u/c$ V, the Rogowski coil has a sensivity of 30 µV/A, the integrator/high-pass filter has a gain equal to 1.2 ≡ 1.64 dB at 50 Hz, and we want to measure AC currents in the following ranges: 1280Arms, 320Arms, 80Arms and 20Arms. According to the previous data, the gains that we should be able to select are: $G_0 = -38.363$, $G_1 = -153.452$, $G_2 = -613.808$, and $G_3 = -2455.2$. A simple method to calculate the resistor values is:

$R_{\alpha 3} = 300 \cdot R_{DS-on} = 300 \cdot 1\Omega = 300\Omega \rightarrow$ we set the smallest value of the R_α resistors to ensure that the value of R_{DS-on} does not have a significant influence on the amplifier gains.

$R_2 = R_3 = 2 \cdot R_{\alpha 3} \cdot (G_3 - G_0)/G_0 = 37799.9 \sim 37800\ \Omega$
$R_1 = -4 \cdot R_{\alpha 3} \cdot (-1 + G_3/G_0)/G_0 = 1970.6 \sim 1970\ \Omega$
$R_{\alpha 1} = R_{\alpha 3} \cdot (G_3 - G_0)/(G_1 - G_0) = 6299.8 \sim 6300\ \Omega$
$R_{\alpha 2} = R_{\alpha 3} \cdot (G_3 - G_0)/(G_2 - G_0) = 1260\ \Omega$

The gains obtained with the calculated values are (theoretical values are shown in square brackets):

$D_3\,D_2\,D_1 = 0\,0\,0 \rightarrow G_0 = -38.3756$ [-38.363]
$D_3\,D_2\,D_1 = 0\,0\,1 \rightarrow G_1 = -153.5025$ [-153.452]
$D_3\,D_2\,D_1 = 0\,1\,0 \rightarrow G_2 = -614.01$ [-613.808]
$D_3\,D_2\,D_1 = 1\,0\,0 \rightarrow G_3 = -2456$ [-2455.2]

designideas

For a non-inverting design, the following method can be used to select resistor values that provide gains $G_0 = 38.363$, $G_1 = 153.452$, $G_2 = 613.808$, and $G_3 = 2455.2$:

The gains obtained with the calculated values are:

$$v_i \geq -\left(\frac{1+R_\alpha/R_{DS-on}}{1+R_2/R_1}\right) \cdot v_F$$

$D_3\ D_2\ D_1 = 0\ 0\ 0\ \rightarrow\ G_0 = 38.3631\ \ [38.363]$
$D_3\ D_2\ D_1 = 0\ 0\ 1\ \rightarrow\ G_1 = 153.4532\ \ [153.452]$
$D_3\ D_2\ D_1 = 0\ 1\ 0\ \rightarrow\ G_2 = 613.8139\ \ [613.808]$
$D_3\ D_2\ D_1 = 1\ 0\ 0\ \rightarrow\ G_3 = 2455.3\ \ [2455.2]$

About the author

Carlos Castro-Miguens received the Electronic Engineering degree from Vigo University, Spain. He is currently employed as associate professor of the Electronic department at Vigo University. His primary interests are in power electronics (dynamic modelling and control of power converters, design of magnetic components for power converters), design of embedded systems and signal processing.

Avago Tech Note: Strain sensing using optical phase interrogation technique with polymer optical fibre   By Avago Technologies

This technical note is intended to give integrators an introduction to optical phase interrogation (OPI) technology, and a basic understanding of how a sensing solution can be used together with polymer optical fibre (POF).

Principle

If we couple a modulated signal into a POF (Figure 1) and subject the POF to strain, the signal will experience a phase shift (Figure 2). The amount of phase shift scales linearly with the amount of strain (Figure 3).
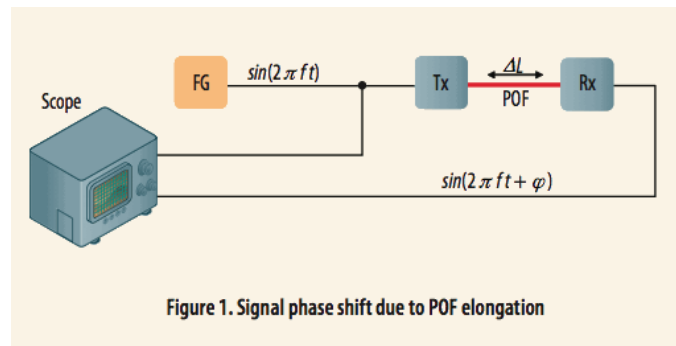

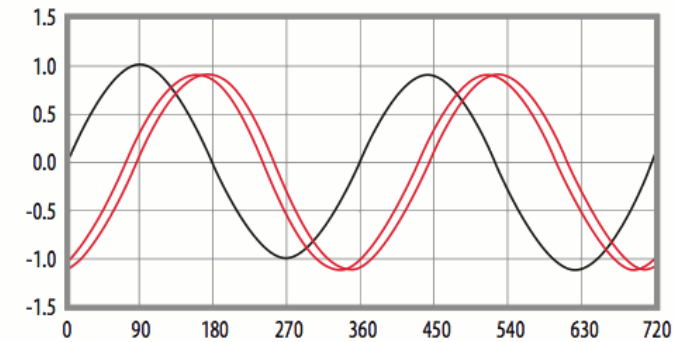Figure 1. Signal phase shift due to POF elongation

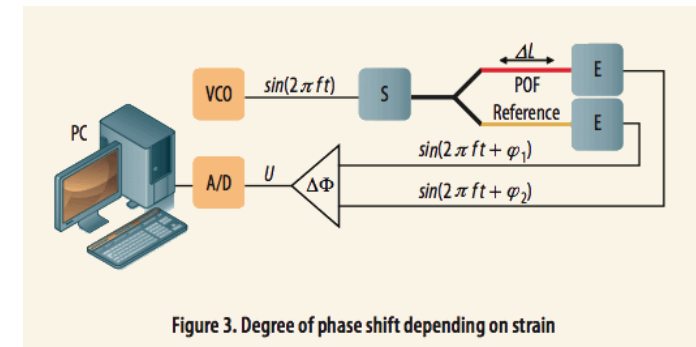Figure 2. Measuring phase shift with phase comparator

Figure 3. Degree of phase shift depending on strain

By splitting the modulated signal into a measuring fibre subjected to strain, and a reference fibre not subjected to strain, and subsequently comparing the two signals over a phase com-

designideas

parator, we can determine the amount of strain the sensing POF is experiencing.

The optimal workpoint is at 90° phase difference between the reference and sensing fibre where the phase comparator is working in a linear region. (Figure 4)
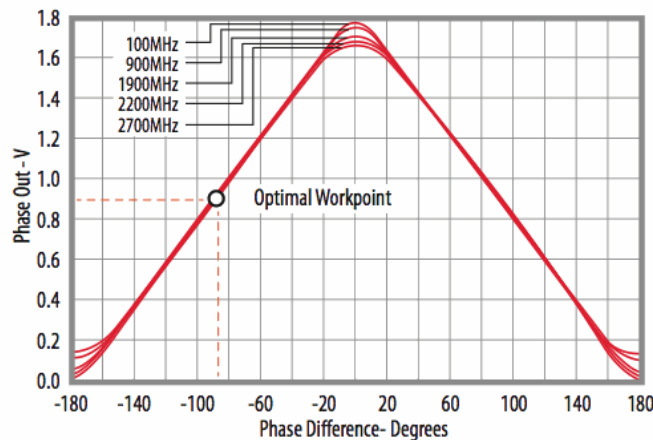

Figure 4. Working point of the phase comparator

Plastic optical fibre characteristics

Made out of polymer (Figure 5), POF offers a comparably high elasticity. Most POF can be stretched more than 5% and remain within the elastic range (Figure 6).
This translates into a wide potential dynamic range of the technology. The large dimension of the fibre makes it easy to handle (Figure 5).

POF is used in a variety of industrial and automotive applications where it has proven its robustness. In addition to its robust characteristics, POF also offers complete EMI/ EMC immunity.
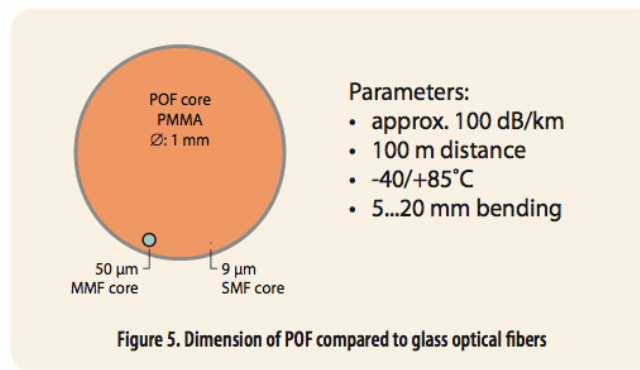

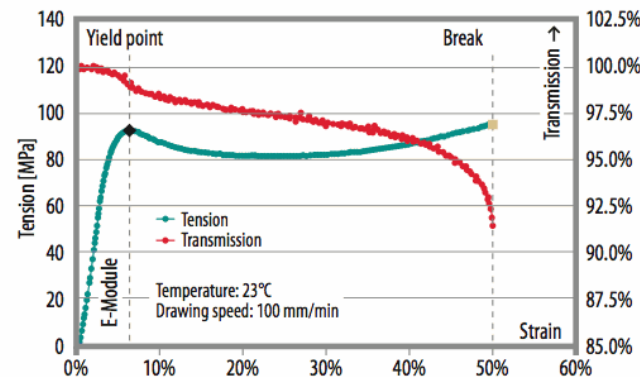Figure 5. Dimension of POF compared to glass optical fibers

Figure 6. Fiber attenuation (transmission) vs strain

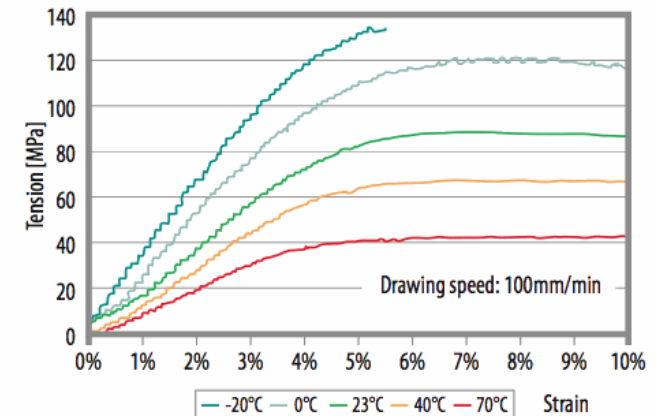As can be seen in Figure 7, the elastic properties of POF remains over a considerable temperature range.

Figure 7. Elastical range remains considerable over a wide temperature range.

*This Note (**click below** to download the complete note in pdf form) continues by considering the resolution achievable with POF sensing; the Dynamics of applying force to fibre, and how a practical measurement setup may be configured; the sensitivity to be expected; and temperature compensatio;*
Optical phase interrogation with POF offers an easy to handle and integrate optical strain sensing solution. The robustness and flexibility of POF are advantages that are evident in rough environments or applications. The optical phase interrogation principle enables temperature compensated strain measurement solutions for a wide range of applications.

Download PDF of Article

productroundup

RS-232 transceivers eliminate level shifters

Exar's RS-232 (EIA/TIA-232) transceivers are designed to operate from 3V to 5.5V supplies. The XR32220, XR32430 and XR32431 include an adjustable low voltage logic interface, via a VL pin, hat simplifies their use in low voltage and multi-voltage systems, used to adjust the transceiver's logic output levels and input thresholds for compatibility with lower supply voltage logic. The VL range is 1.65V to 5.5V. The adjustable low voltage interface eliminates the need for a level shifter/translator between the transceiver and UART or MCU.
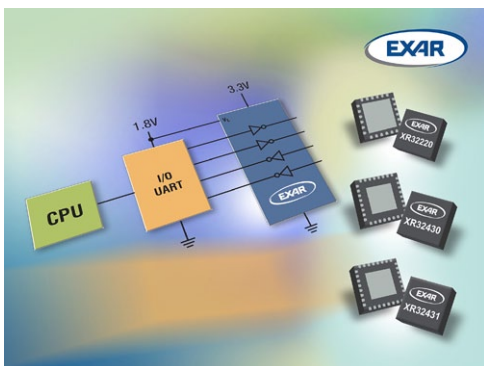
Complete article, here ▶

Powerline modem IC for worldwide standards

Renesas' third-generation OFDM powerline (PLC) modem provides the flexibility to support any PLC protocol standard, such as PRIME1.3.6/1.4 and G3, for all global frequency bands including CENEL-EC A, FCC and ARIB. The new modem device integrates an enhanced MAC controller supporting large scale network hopping and routing as well as a high performance digital signal processor (DSP) with special instructions for PLC, covering the physical layer (PHY) and real time processes of the media access protocol (MAC) implementation.
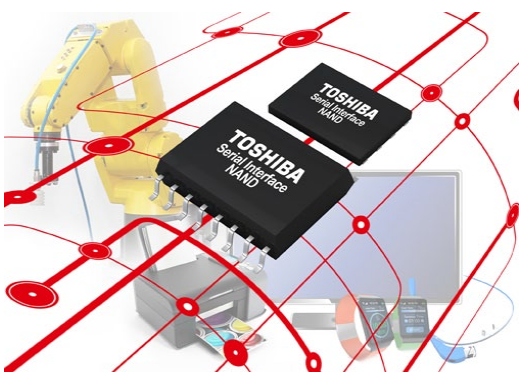
Complete article, here ▶

Serial interface NAND flash for embedded boot

Toshiba Electronics Europe's 24nm SLC NAND flash memory for embedded applications has Serial Peripheral Interface (SPI) and was developed for large but low cost memory to use in, for example, boot-memory in place of NOR flash. Designers might be using, for example, more than one package of 128 Mbit serial NOR flash for this purpose; Toshiba suggests replacing that with a single package of 1 Gbit or larger, to store boot routines and other data. The new line-up spans densities of 1Gbit, 2Gbit and 4Gbit.

Complete article, here ▶

Super-junction power MOSFETs at 1500V rating

A family of power MOSFETs from STMicroelectronics, MDmesh K5, devices are the first to combine the benefits of super-junction technology with a drain-to-source breakdown voltage of 1500V. They claim the lowest on-resistance (Rds(on)) per area and the lowest gate charge (Qg), resulting in the industry's best FoM (Figure of Merit). STW12N150K5 and STW21N150K5, offer maximum drain-to-source currents of 7A and 14A, respectively, with gate charge as low as 47 nC (STW12N150K5) or on-resistance as low as 0.9Ω (STW21N150K5).

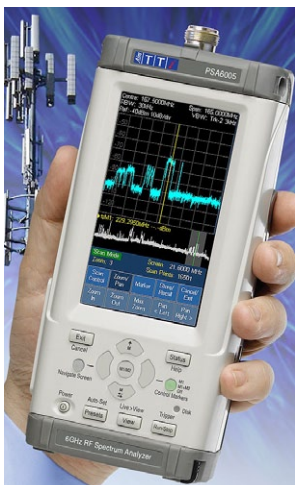1500V MDmesh K5 MOSFETs
Industry's best $R_{DS(on)}$ per area and FoM

Complete article, here ▶

Handheld spectrum analyser captures 200k points

The PSA Series 5 RF spectrum analysers from Aim-TTi have been enhanced to include high resolution capture of signals over a wide span. Option U02 now includes an extra facility called Scan Mode. In scan mode a narrow RBW(resolution bandwidth) can be set whilst retaining a wide span because all data points (up to 210,000) are written to a file. When the scan is completed a compressed version of the data is displayed with pan and zoom controls enabling any portion of the data to be observed in detail. The Series 5 includes the 3.6 GHz PSA3605 and the 6 GHz PSA6005.

Complete article, here

Low cost dashboard combines three displays

A free programmable instrument cluster, a head-up display and an infotainment system with touchscreen, all driven by one dual-core processor; SoC designer Socionext is offering such a solution. The three displays are connected to the control unit through independent APIX

links. This low-cost concept meets with growing demand to connect smartphones with the vehicle, the chip company said. Through a MirrorLink integration the system benefits from turning the smartphone, with its significant computing resources, into an automotive application platform.

Complete article, here

In-car video link at 12Gbps for high resolution

Inova Semiconductors has announced its APIX3 multi-channel SerDes (serialiser/deserialiser) technology for video and data communication in vehicles. It aims to enable a 4x speed-up in video transmission for efficient, cost-effective next-generation automotive infotainment. APIX (Automotive Pixel Link) is a multi-chan-

nel technology for high resolution in-car video applications. The latest APIX3 version supports transmission at up to 6 Gbps over a single twisted pair (STP) cable and up to 12 Gbps over a quad twisted pair (QTP) connection.

Complete article, here

Shunt-based module measures up to 375A

Combining the Sendyne SFP102 sensing IC with a Vishay 100-μΩ shunt in a moulded package, the SFP102MOD measures up to 375 A peak with an accuracy of ±0.25% over the device's entire temperature range of -40°C to +125°C. The SFP102MOD achieves a resolution of 45 μA. When attached to properly sized cables/bus bars,

the SFP102MOD operates with 200 A of continuous current, producing less than a 45°C temperature rise. It features built-in Coulomb counting (charge accumulation), with separate counters for charge, discharge, and total Coulombs.
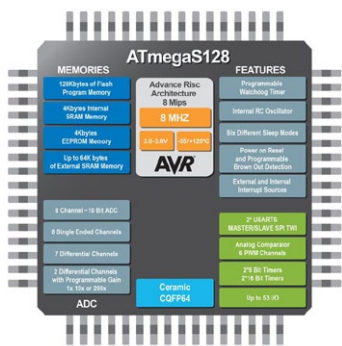
Complete article, here

productroundup

Rad-tolerant megaAVR MCU

Atmel ATmegaS128 AVR microcontrollers are now produced in space-grade quality, including latch-up immunity, ceramic packaging and extended temperature range. AtmegaS128 delivers full wafer lot traceability, 64-lead ceramic package (CQFP), space screening, space qualification according to QML and ESCC flow and total ionising dose up to 30 krad (300 Gy Si) for space applications. The ATMegaS128 is "latch up" immune thanks to a dedicated silicon process: SEL LET > 62.5Mev at 125°C, 8 MHz/3.3V. SEU to heavy ions is estimated to 10^{-3} error/device/day for Low Earth Orbit applications.
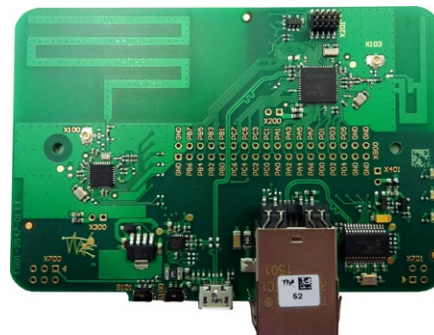
Complete article, here

6LoWPAN IoT gateway wireless router

From distributor RS, the Weptech (Landau, Germany) 6LoWPAN IoT Gateway provides an affordable open-source-based solution for connecting 6LowPAN-based IoT networks to the Internet. It functions as a border router in a 6LoWPAN-based network and connects a wireless IPv6-based network to the Internet. The board facilitates the routing procedures necessary to integrate an IPv6 mesh network comprising small wireless low-power devices into the global IP network. It enables users to connect up to 32 6LoWPAN 'child' nodes to the network.

Complete article, here

Low-power 1080p camera reference design

ON Semiconductor, GainSpan and GEO Semiconductor are working on products for emerging IoT markets, combining ON Semiconductor's image sensors, GEO's image signal processing technology and GainSpan's low power Wi-Fi solutions. A highly optimised IoT video reference design is the trio's first collaboration. The GS-AR0330-Based Full HD Video, available via GainSpan and its distributors, targets smart 1080p video streaming over Wi-Fi. Through wireless connectivity, it can interface seamlessly with smartphones that use either iOS or Android operating systems. The solution comprises all of the hardware and software needed for engineers to add video streaming capabilities into their IoT-based designs. The video reference design is accompanied by a complete software suite, plus a series of mobile application programming interfaces (APIs).

Complete article, here

ADAS surround view development kit

Renesas' ADAS Surround View Kit is intended to enable quick time to market for automotive system manufacturers; the kit is an extension of Renesas' ADAS Starter kit itself designed to be used in a wide spectrum of applications. The ADAS Surround View Kit combines automotive cameras from Integrated Microelectronics Inc. and multiple high-speed gigabit multimedia serial links (GMSL) from Maxim Integrated Products, on a miniature automotive chassis. This eliminates the need for system manufacturers to source and set up all these specific automotive components.
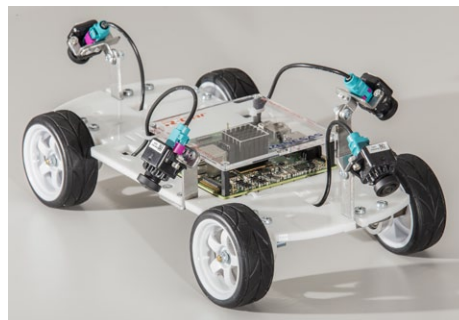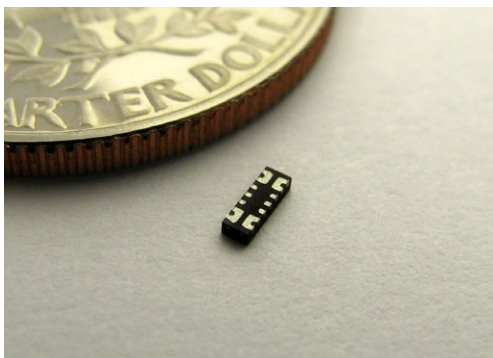
Complete article, here

productroundup

Reverse-blocking 7.8 mΩ/9A power switch

In Silego Technology's range of single-channel, self-contained, reverse-blocking integrated power-switches, the SLG59M1600V is optimised for high-current, low-voltage power-rail distribution, power-rail sequencing, or any other power-rail application where power flow from load to source cannot be tolerated. With an internal charge pump, output voltage discharge circuitry, user-adjustable inrush current, thermal protection, and ON/OFF control, the SLG59M1600V is a completely self-contained integrated power switch.
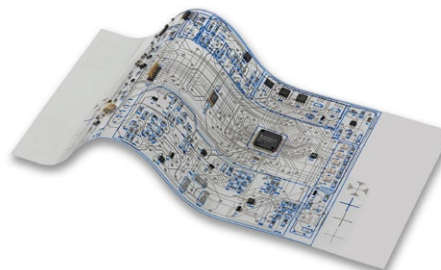
Complete article, here

Flexible printed sensor solutions from Molex

Molex has expanded its printed electronics portfolio with the recent acquisition of Soligie. Custom Soligie products provide a robust and economical alternative to a rigid PCB or copper flex circuits. Soligie sensor solutions can be applied in measuring temperature, shock and humidity, physiological monitoring, environmental and biochemical sensors, and virtually any sensor product requiring a thin, flexible electronic form factor. Designs start with a low cost substrate onto which functional components are added using conductive silver ink to form the circuitry.
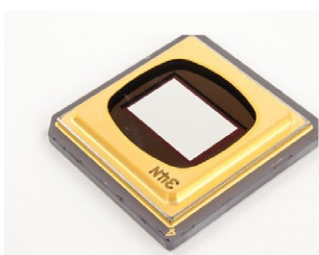
Complete article, here

Fastest, highest-resolution DLP chipset

With more than 4 million micromirrors, and presented as its highest speed and resolution chipset for 3D printing and lithography applications, TI's DLP9000X digital micromirror device (DMD) and the DLPC910 controller offers developers more than five times the speed at continuous streaming compared to the existing DLP9000 chipset. The DLP9000X DMD delivers the highest streaming pixel speed in the TI DLP Products portfolio at over 60 gigabits per second. Example application areas for the DLP9000X include 3D printing, direct imaging lithography, laser marking, LCD/OLED repair and computer-to-plate printers, as well as 3D machine vision and hyperspectral imaging.
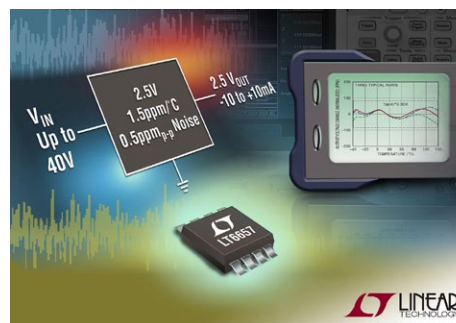
Complete article, here

Lowest-drift bandgap voltage reference

LT6657 is a family of ultra-stable bandgap voltage references that exhibits less than 1.5ppm/°C of temperature drift. The device has only 0.5ppm p-p of low frequency noise, less than 30 ppm of long term drift and 35 ppm of thermal hysteresis. It is fully specified for –40°C to 125°C and was designed for high performance instrumentation, test equipment and automotive systems. The LT6657's buffered output can source and sink up to 10 mA, and it can operate on a supply voltage from 50 mV above the output, up to 40V, and with a supply current of only 1.2 mA.

Complete article, here

Under the radar

Several years ago we received reports from a customer that our marine radar units would sometimes shut down when the vessel travelled under high-tension power lines that crossed the waterways. The customer was in another country, so it was difficult to troubleshoot the problem directly.

We came up with several theories as to why this was occurring and tested them in the lab. We used an EMI test bench, which induced currents in the wiring between the radar head and the control unit, but no shutdown was observed. We made several software changes in the radar, thinking that the software was not filtering the hardware shutdown signal from the control unit well enough, but this did not solve the problem. Finally, one of the technicians recommended that we mount the radar on the back of a pickup truck and drive under a local 345 kV line to see if the problem occurred. No one expected to replicate the problem but we decided to go ahead with the plan. We executed the plan one morning, driving under the line several times with no problems. As we stood under the line, I commented to the others that I couldn't hear the line "hissing," and the line might not be live. The other engineer involved called the vice president of the power company and he put us in touch with dispatching, who told us the line indeed was not activated, but that it would be the following Monday.

Monday morning we were out again, slowly driving closer to the line. As we were about 200 feet away from the centre line, the radar crashed! We tried again several times and the result was the same each time. We also tried another unit, but it did not fail. After much head-scratching, we were puzzled as to why this was happening. The unit was inside a metal enclosure, with a rotating metal waveguide style antenna on top. All the connecting wires were shielded. The radar operates at an X-band frequency, which should be too high to see interference from the power line and even if it did see interference, that shouldn't shut the unit off.

As I was driving to work the next morning, I had a thought—what if the radar antenna itself was not bonded to the frame of the radar? The high voltage field could induce a voltage on the antenna, and if it were not bonded, then a spark could jump to the internal waveguide and subsequently the main circuit board and cause the processor to reset.

I rushed to the lab and put a multimeter across the metal on the antenna to the ground of the radar. No connection! The antenna was designed to come off for shipping, but the screws that held it on were insulated from ground. The antenna connection was a simple rotary waveguide fitting without screws. The waveguide faces were designed with microwave traps that would slide into position facing one another when the antenna was attached. However, there was no guarantee of a low frequency connection across the mating waveguide faces.

I did a quick fix by placing conductive foam between the antenna metal frame and the top of the internal waveguide. This resulted in a grounded antenna when it was bolted in place. I also took the unit that did not fail and placed a small piece of Kapton tape between the faces of the waveguide. We took the failing unit back out and no longer saw the problem, whereas the previously non-failing unit now failed because of the tiny spark gap.

The field repairs were easy—simply remove the antenna and place a small adhesive conductive foam pad to contact with the metal antenna body, on top of the rotary waveguide. No more complaints from the customer!

Larry Morse *has been involved with electronics since the seventh grade, and subsequently went into electrical engineering, working in the field for 40+ years. He has been a generalist, with experience in analogue, digital, software, DSP, and RF, and his latest speciality has been digital signal processing using FPGAs. His hobbies include amateur radio, photography, and woodworking.*

EDN europe

CONTACTS

PUBLISHER
André Rousselot
+32 27400053
andre.rousselot@eetimes.be

EDITOR-IN-CHIEF
Graham Prophet
+44 7733 457432
edn-editor@eetimes.be

Patrick Mannion
Brand Director EDN Worldwide

CIRCULATION & FINANCE
Luc Desimpel
luc.desimpel@eetimes.be

ADVERTISING PRODUCTION & REPRINTS
Lydia Gijsegom
lydia.gijsegom@eetimes.be

ART MANAGER
Jean-Paul Speliers

ACCOUNTING
Ricardo Pinto Ferreira

european
business press

SALES CONTACTS

Europe

Daniel Cardon
France, Spain, Portugal
+33 688 27 06 35
cardon.d@gmail.com

Nadia Liefsoens
Belgium
+32-11-224 397
n.liefsoens@fivemedia.be

Nick Walker
UK, Ireland, Israel,
The Netherlands
+44 (0) 1442 864191
nickjwalker@btinternet.com

Victoria & Norbert Hufmann
Germany, Austria,
Eastern Europe
+49 911 93 97 64 42
sales@hufmann.info

Monika Ailinger
Switzerland
+41-41-850 4424
m.ailinger@marcomedia.ch

Andrea Rancati
Italy
+39-02-284 6716
info@silvera.it

Colm Barry & Jeff Draycott
Scandinavia
+46-40-41 41 78
jeff.draycott@womp-int.com
colm.barry@telia.com

USA & Canada

Todd A. Bria
West
+1 831 477 2075
tbria@globalmediasales.com

Jim Lees
PA, NJ & NY
+1-610-626 0540
jim@leesmedia.com

Steve Priessman
East, Midwest,
South Central
& Canada
+1-630-420 8744
steve@stevenpriessman.com

Lesley Harmoning
East, Midwest,
South Central
& Canada
+1-218.686.6438
lesleyharmoning@gmail.com

Asia

Keita Sato
Japan
+81-3-6824-9386
MIshida@mx.itmedia.co.jp

Grace Wu
Asian Sources Publications
Asia
(886-2) 2712-6877
wug@globalsources.com

John Ng
Asian Sources Publications
Asia
(86-755) 8828 – 2656
jng@globalsources.com